Low T_c Superconductive Circuits Fabricated on 150-mm-Diameter Wafers Using a Doubly Planarized Nb/AlO_x/Nb Process

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Abstract—**We have used a doubly planarized all-refractory technology for superconductive electronics (DPARTS) process to fabricate mixed-signal circuits that have more than 200 junctions per circuit and operate at 2 GHz. A 150-mm-diameter wafer can produce more than 400 chips, each 5 mm on an edge. The junctions had a *critical* current density of 1.7 kA/cm^2. The wafers were evaluated at room temperature, both in- and post-process. In-process testing was used to detect parameter shifts during processing, while post-process testing used an automated testing station to test more than 3500 structures across each completed wafer and thus establish a large set of statistical data for studying the spread and targeting of parameter values. The circuits were fabricated in a class-10 clean room in which 0.25 μm CMOS and CCD devices were also produced. The DPARTS process could also be used for sub-μm fabrication, as it includes optical lithography with an i-line stepper; chemical-mechanical planarization at two levels; a self-aligned via process; and dry, anisotropic etching for all metal etching and via definition steps. The use of 150-mm-diameter wafers ensures that this process will be able to exploit technological advances in the standard silicon tool set as improvements become available. The results demonstrated here are a necessary precondition to yielding large volumes of superconductive electronic circuits containing devices with sub-μm dimensions.**

I. Introduction

To compete with silicon processes, present and future, superconductive electronics must distinguish itself by demonstrating speeds far beyond what is deemed possible for conventional microelectronics. In the past, such demonstrations were possible using relatively coarse design rules in the fabrication process, however semiconductor-based electronics have advanced so rapidly that now there is a need to reduce the junction capacitance by pushing the junction design rules below 1 μm. This need for tighter fabrication tolerances is likely to continue as silicon continues its steady march towards faster and faster device operation. For superconductive circuitry to outpace the advance of semiconductor-based circuitry, the most advanced silicon fabrication toolset must be exploited fully but fabrication tools are no longer made to be compatible with small wafers: fabrication using wafers of at least 150-mm-diameter is becoming a practical necessity for advanced superconductive electronic processes.

We will first present an outline of the fabrication process, that was originally modeled on the PARTS process developed at IBM.[1] We will end with a brief discussion of testing methods and results. We will not discuss any of the high-speed testing results for circuits fabricated using this process, as these will be discussed in another paper presented in this issue.[2]

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II. Process Description

Figure 1 outlines the process in cross-section. The substrates were 150-mm-diameter silicon wafers with 5.0 kÅ of thermal oxide grown on their surface. The first step in the process was trilayer fabrication, followed by patterning and etching of the counterelectrode. The base electrode was then defined, the barrier was stripped, and the base electrode was etched. A PECVD oxide was then deposited, followed by the first planarization step; in this step the oxide was polished until the counterelectrode surface was revealed. The resulting self-aligned contact to the counterelectrode obviated an additional via etch. The resistors were then defined using liftoff; vias were etched to the base electrode; the wiring layer was deposited, patterned, and etched. This was followed by the second PECVD oxide deposition; the oxide was planarized and vias were etched. Finally the ground plane was deposited, patterned, and etched, and contact pads were defined using liftoff.

We will now describe each of these processes in detail.

A. Trilayer Fabrication

The trilayer was fabricated in a DC magnetron sputtering system equipped with 6" Nb and Al targets. The process proceeded as follows: 1) two wafers at a time were loaded into the system (the vacuum system was not load-locked). 2) The system was pumped down until a pressure of ~1.2×10^{-7} Torr was achieved (overnight). 3) Nb was sputtered at 10 mTorr and 1500 W of power to form a base electrode 1500-Å-thick at a rate of ~1500 Å/min. 4) The wafers were allowed to cool for 1 hour. 5) Al was sputtered at 2 mTorr and 1 kW of power to form an Al layer 60-Å-thick at a rate of ~1000 Å/min. 6) The wafers were allowed to cool for 30 minutes. 7) The wafers were then oxidized for 30 minutes at pressures ranging from 70-130 mTorr, depending on the desired J_c. After oxidation the wafers were pumped down for at least two hours and until a pressure of at least 5×10^{-7} Torr was achieved. 8) Nb was sputtered to form a counter-electrode 2500-Å-thick, 9) the wafers were cooled for 1 hour and then removed from the chamber. Although the platen was water cooled, the wafers were not heatsunk to the platen in any way.

Following trilayer fabrication the wafers were cleaned in a

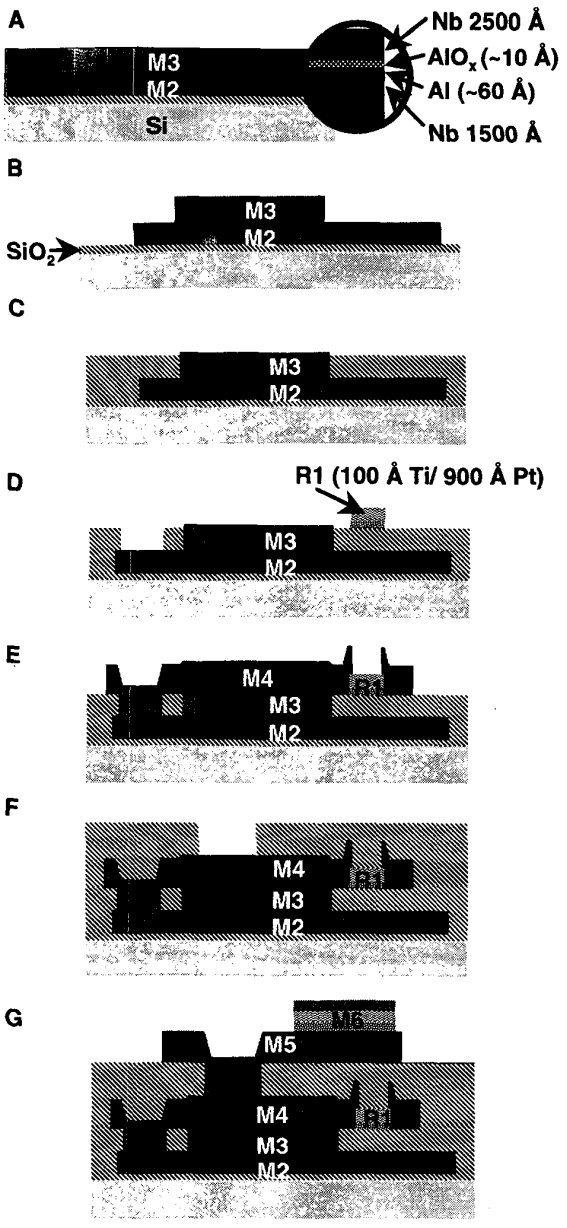

Fig. 1. The DPARTS process included six metal layers, two via layers, and two planarization steps: one before R1 deposition and the other before M5 deposition. A) The trilayer was deposited, B) the counter electrode was etched, the barrier was stripped from regions over the base electrode, and the base electrode was etched, C) the oxide was deposited and the wafers were planarized until contact to the counterelectrode was opened up, D) resistor metal was deposited and lifted off, and vias were etched to contact the base electrode, E) the wiring layer was deposited and etched, followed by F) another oxide deposition, planarization, and via etch, G) finally the ground plane was deposited and etched, followed by the Ti/Pd/Au contact pads which were patterned using liftoff. There is no "M1" layer.

megasonic rinser with a mild detergent solution, followed by cleaning with deionized water in a spin-rinser dryer: this process was required by laboratory protocol, but is presumed not to be critical.

B. Photolithographic Processing

The patterns were defined on a GCA i-line 5x-reduction 365-nm-illumination stepper. The reticles were fabricated by Rockwell Semiconductor Systems to a tolerance of 0.25 μm. We discovered that even in the class-10 cleanroom, defect-free fabrication required frequent cleaning of the reticles to remove dust.

The field size of 15.5 mm was sufficient to fit nine $(5\text{-mm})^2$ chips. As many as 4 separate reticles were stepped onto any given wafer to accommodate multiple circuit designs in a single fabrication run. Most reticle sets also incorporated two wiring reticles for the M4 layer; these reticles differed in which designs they connected to the contact pads and were stepped alternately across the wafer. This effectively doubled the number of designs that could be fabricated on each wafer for the cost of only a single extra reticle.

For all processing steps other than the resistors and pads, the photoresist used was Shipley SPR-511A positive tone photoresist, applied at 3750 RPM and then baked for 60 seconds at 95°C to give a 1.2 μm-thick layer; we used hexamethyl disiloxane (HMDS) vapor to prime the wafers at 150°C for 30 seconds prior to resist coating; this improved adhesion of the photoresist to the substrate. The exposure dose of 155 mJ/cm^2 gave a CD within +/- 0.1 μm of the nominal value, as determined by measurements using calibrated electron and optical microscopes. After exposure, the wafers were baked at 95°C for 60 seconds and developed using Shipley MFT .245, for two sequential 60-second puddle-develop steps. Finally the resist was hardbaked at 115°C for 60 seconds.

An image-reversal process with AZ5214-E-IR photoresist was used for liftoff processing of the resistors and contact pads. The wafers were primed as before, then ~8 ml of photoresist was spun on in the case of resistors (pads) at 3900 (3000) RPM to give a resist thickness of 1.4 (1.6) μm; the wafers were then soft-baked at 95°C for 60 seconds. The photoresist was exposed to a dose of 30 (40) mJ/cm^2 and then hardbaked at 110°C for 45 seconds. The photoresist was then flood exposed at a dose of 300 mJ/cm^2 and developed using two puddles of AZ-327 developer, for a total of 120 seconds. This process served to give a vertical resist-sidewall profile, and allowed for clean liftoff.

C. Niobium Etching

The etching process was virtually identical for the counter- and base-electrodes, as well as for the wiring layer and ground plane. All of these steps used a load-locked reactive ion etch (RIE) chamber with SF_6 gas at 50 W of power, 25 mTorr of pressure, and a platen temperature of 50°C (helium backside cooled) in a load-locked chamber. The end of the etch was determined by using fluorescence spectroscopy (fluorescence intensities of both product and reactant peaks were monitored). The wiring layer was overetched by 90 seconds to assure adequate removal of niobium stringers from

the edges of the resistors. The etch was observed to proceed from the outside of the wafer towards the center, so the outer edges were overetched by 10-20 seconds relative to the wafer center. This process has been observed to be sensitive to chamber conditions, but in contrast to past experiments, which have suggested frequent cleaning is necessary for reproducible results,[3] we have had most success when the chamber is not cleaned or allowed to come to atmospheric pressure for long periods of time. All etches were preceded by the etch of two monitor wafers for the purpose of chamber wall passivation.

D. Photoresist Stripping

The photoresist was removed after both metal and oxide etching using ACT-935 photoresist stripping solvent. Immersion in ACT-935 at 75°C for 30 minutes was sufficient to remove the resist and any additional residues. After photoresist removal, the wafers were cleaned using deionized water in a dump-rinser and spin-rinser dryer. ACT-935 was found to be an acceptable substitute for plasma ashing of photoresist residue; we thus avoided having to expose niobium to oxidizing plasmas. Without this stripping step, substantial metal residue remained on the wafers in the form of grass-like pillars all over the etched areas; we therefore conclude that niobium does etch at some slow rate in ACT-935, and indeed this slight etch is critical to the success of our niobium dry-etch process.

E. Barrier Removal

The barrier was removed by a 90-second immersion in a fresh bath of 15% phosophoric acid at 50°C. After etching, the wafers were cleaned in a dump-rinser and spin-rinser dryer using deionized water.

F. Oxide Deposition

The oxide was deposited in a PECVD chamber using a combination of 2% SiH_4 (in helium) and N_2O in a ratio of 9:4 at 900 mTorr pressure and 20 W of power. The chamber was load-locked, and the platen was kept at 150°C. The oxide deposition rate was ~400 Å/min, and the chamber underwent a cleaning step consisting of a PDE-100 (82.5% CF_4 and 17.5% O_2) plasma at 250 W and 300 mTorr after every 20 minutes of deposition. For the I2 layer, 6000 Å of oxide was deposited, while for the I3 layer, 7500 Å of oxide was deposited. Electron microscope inspection revealed that this oxide was permeated with voids, and tended to crack when crossing over the metal steps. Planarization subsequently improved the oxide surface and acted to seal these cracks. Breakdown fields of > 5 MV/cm were routinely realized using this oxide as an insulator, even over test structures including complicated topography underneath the planarized layer; we therefore concluded that this process was adequate for the given purpose.

G. Planarization

Chemical-mechanical planarization (CMP) was used to form self-aligned contacts to the counterelectrode. We used a Rodel IC-60 pad and ILD-1300 slurry, also from Rodel, dispensed at a rate of 100 ml/min. The slurry pH was ~10.7, and the pad wafer temperature was measured to be 30°C during the polish. The wafer was pressed against the polishing pad with a pressure of 4 psi, and a back pressure of 0.5 psi was applied to the wafer, in order to bow the wafer out slightly and thus to reduce the tendency of the wafer edges to polish faster than the wafer center. This resulted in a polishing rate of 850Å/min (+/-6%* variation from run to run; +/-6% variation across the wafer). To achieve accurate polish endpoint, the polish was typically done in several steps which progressively approached the desired final oxide thickness. After each polish the oxide thickness was determined using spectral reflectometry, and thus the remaining polish depth was determined. Typically the process required between two and four polish-measurement cycles.

After CMP the wafers were cleaned in a megasonic station with a mild detergent solution, as required by laboratory protocol, followed by a deionized water rinse in a spin-rinser dryer.

H. Resistor Metal Deposition

The resistor metal layer was deposited by electron-beam evaporation of 100 Å of Ti, followed by 900 Å of Pt onto a rotating platen that could hold up to three wafers at a time. Typically one position was occupied by a dummy wafer, used to monitor the post-process sheet resistance of the film, while the other two positions could be used for process wafers. The deposition time was controlled by using a water-cooled quartz-crystal microbalance to measure the metal thickness.

The room temperature sheet resistance varied from run to run by 6%, while the cross-wafer sheet resistance varied by 3%. Recent improvements in the tool used for evaporation have lowered the run-to-run sheet resistance variation to 3%. The low-temperature sheet resistance was targeted at 0.6 Ω/□, but was substantially more variable than the room temperature sheet resistance: the resistance ratio from 296 to 4.2 K was ~ 4.5 and was inversely correlated to the sheet resistance, thus the variances of the resistance ratio (~ 7 %) and the room temperature sheet resistance add simply, rather than in quadrature, to give a 10% variation in the low temperature sheet resistance.

Liftoff of the metal was achieved by immersion in acetone, followed by a 10-minute immersion in ACT-935, the same solvent used for photoresist stripping. The resistors were observed by atomic force microscopy and secondary-electron

* All specified errors refer to one standard deviation of a presumed statistically normal distribution. Straight forward calculations show that acceptable (10%) yields of circuits with more than 300 devices require circuits to be designed with tolerance to variations in device parameter values of +/- 2.5 times the standard deviation of the process.

microscopy to have raised areas at their edges, probably resulting from the liftoff process—this effect was ignored as it was not found to impact the process yield.

We have demonstrated that liftoff results in a ~1.5 μm process runout: electrical linewidth measurements of the resistors indicate that they are narrower than their nominal width. This effect is entirely due to contamination of the resistor edges by outgassing from the photoresist during metal deposition, and can be eliminated by moving to an etching-based resistor-definition process.[4]

I. Oxide Etching

The vias to the base electrode and wiring layers were etched in a RF RIE system. The etch recipe consisted of 800 mTorr of 200/20/20 sccm $Ar/CF_4/CHF_3$, using 150 W of power and a water-cooled stage at -20°C. The etch rate was ~3000 Å/min, and the etch included a 25% overetch. Because stacked vias were allowed in this process, the etch depth for the second via etch was the sum of the via depths, which resulted in a long overetch of the some of the vias. Stacked vias are no longer permitted by the design rules for this process.

J. Niobium Deposition

The wiring layer and ground plane were deposited by argon sputtering. Prior to deposition the surface received a 5-minute-long ion-beam clean with a current density of 1.5 mA/cm^2 and a beam energy of 500 eV in order to remove the barrier and native oxide from the M2 vias and promote adhesion of the niobium to the oxide surface. The metal was then deposited using an argon plasma at 2.9 mTorr, with 2.5 kW of power, at a rate of ~200 Å/min. The ground plane deposition (4000 Å) was split into two halves with a 20-minute-long cooldown period in between, to avoid overheating the wafers.

K. Contact Pad Deposition

The contact pads were deposited by electron-beam evaporation, and consisted of 300 Å Ti, 3600 Å Pd, and 500 Å Au. The metal pattern was then lifted off in acetone.

III. Process Testing Methods

The fabricated devices were tested both in- and post-process with test structures designed to investigate three categories of quality control: 1) process control using test structures that measure oxide breakdown voltage and leakage current, metal sheet resistance,[5] and electrical linewidth.[6] 2) process yield using test structures that look for shorts or opens in long via strings, interdigitated line/space arrays, and long junction strings, 3) device parameter targeting using test structures for determining J_c (both at 300K[7] and 4.2 K), sheet resistance of the resistor layer, and inductance. The testing was performed using an automated wafer probing station that was able to test ~3500 test structures distributed across a 150-mm-diameter wafer in a few hours. The test data was imported into a database and tracked over time as a means of statistical process control.[8]

IV. Conclusions

The central result of this work is the demonstration of a process for the fabrication of 1.7 kA/cm^2 Josephson junction electronics on 150-mm-diameter substrates. This process has demonstrated acceptable yield for circuit complexities of up to 400 Josephson junctions and 500 resistors per chip. Because this process incorporates lithography using an i-line stepper, dry etching of all metal layers, planarization, and a self-aligned via process for making contact to the junctions, it is well-suited to fabrication of sub-μm Josephson junctions.

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