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We designed, fabricated, and tested a one-dimensional array of superconducting-nanowire single-photon detectors, integrated with on-chip inductors and resistors. The architecture is suitable for monolithic integration on a single chip operated in a cryogenic environment, and inherits the characteristics of individual superconducting-nanowire single-photon detectors. We demonstrated a working array with four pixels showing position discrimination and a timing jitter of 124 ps. The electronic crosstalk between the pixels in the array was negligible. © 2013 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4823542]

Superconducting nanowire single-photon detectors (SNSPDs) have applications in a number of fields, such as quantum key distribution,[1] characterization of quantum emitters,[2] integrated circuit testing,[3] distributed fiber sensing,[4,5] medical diagnostics,[6] light detection and ranging (LIDAR),[7] and space-to-ground communications.[8] Many of these applications would benefit from the ability to simultaneously resolve photon arrival spatially and temporally, for example, to increase throughput rates in a communications system or to take fluorescence images of biological samples. Compared with other types of infrared single photon detectors,[9] SNSPDs made from NbN have superior characteristics, including detection efficiencies of 76%,[10] a wide response spectrum that spans wavelengths of $0.5 \sim 5\,\mu m$,[11] dark count rates below 100 counts/s, count rates above 100 MHz,[10] and timing jitter less than 50 ps. In this paper, we describe an array architecture which is capable of spatial and temporal resolution and demonstrate a working four-pixel array with negligible electrical crosstalk.

Reading out several SNSPDs at once is a complex task with two primary challenges that need to be overcome. First, the output signals must be amplified above the electrical noise level of the readout and second, the SNSPD's signals must be distinguished from one another. Since standard semiconductor electronics do not work at cryogenic temperatures, amplifying the millivolt-scale, nanosecond-scale SNSPD output pulses typically require RF lines running from room temperature to the cold sample. To distinguish between detector pixels, past spatially resolved arrays have carried each SNSPD's signal on a separate RF line and thus required readout electronics listening to each line.[12] Unfortunately, finite cooling power of the cryocooler limits the number of RF cables that can be used to carry output signals from the sample. Thus, the signals from any array of SNSPDs with more than a few elements would ideally be multiplexed onto a limited number of output lines. There have been other SNSPD array designs used for photon number resolution,[13,14] but these designs lacked spatial resolution. Recently, a time-multiplexing method using transmission lines was proposed,[15] however, segments of long transmission lines would be needed to separate the pulses, which makes implementing this method on a single monolithic chip difficult. Using a different approach, two groups implemented single-flux-quantum (SFQ) logic circuits to read out isolated SNSPDs.[16,17] This method could potentially support arrays with many elements, because SFQ circuits can multiplex signals digitally.[18,19] Nevertheless, both the readout architecture and the fabrication of SFQ circuits are complex, requiring custom Josephson-junction-based SFQ chips fabricated separately from SNSPD devices.

We have developed an integrated method of analog readout that encodes the location of the photon arrival in an SNSPD array into the amplitude of the output pulse. This encoding is possible because the amplitude of an SNSPD output pulse depends only on circuit parameters and does not relate to the energy or the number of the incident photons. The diagram in Fig. 1(a) depicts how the array works. When one pixel of the array is fired due to a photon absorption or dark count, the current biased through that element is split to the two outputs. The two outputs carry their respective pulses to room-temperature electronics, where their amplitudes are subtracted one from the other. The peak value of this differential signal then uniquely identifies which pixel fired. Since each pixel works the same way as a typical SNSPD, the array inherits the characteristics of the constituent SNSPDs. Additionally, all circuit components are passive and fabricated on-chip. Only two RF coaxial lines and one DC bias line were used to operate the array, allowing for monolithic integration of the entire array on a single chip.

Fig. 1(c) shows the schematic diagram of a four-pixel array. Each pixel consisted of (1) an SNSPD, (2) a series inductor L_s, and (3) a series resistor R_s. The four pixels were connected in parallel through current-splitting inductors L_p. The output signals generated by the pixels were delivered to RF lines on either side of the array, and are denoted as the voltages V_L and V_R. The pixels were designed to be biased

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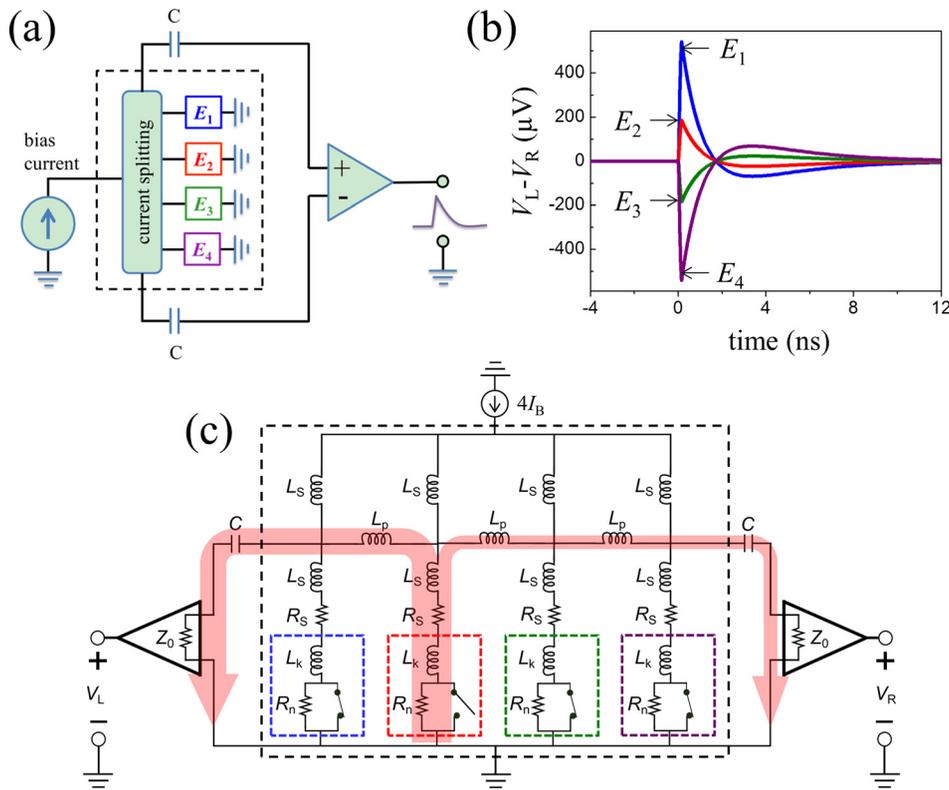
FIG. 1. Four-pixel current-splitting array. (a) Operational diagram of the array. All elements within the black-dashed box are parts on-chip. E_1 (blue), E_2 (red), E_3 (green), and E_4 (purple) are the four pixels. Their colors correspond to the pulses and the equivalent circuit in the other subfigures. (b) Electrothermal simulation of the $V_L - V_R$ for detection events in pixel E_1 (red), E_2 (blue), E_3 (green), and E_4 (purple). The simulation parameters were $R_s = 200\,\Omega$, $Z_0 = 50\,\Omega$, $L_s + L_k = 400\,nH$, and $L_p = 50\,nH$. (c) Schematic diagram of the current-splitting array. The current flow to the output when E_2 was triggered is shown as an example. The widths of the arrows represent the amplitude of the current qualitatively.

through the L_s, but could be also biased through the output ports by using a bias-tee before the amplifier (see the supplementary materials[20]). To prevent the diverted current from leaking out through neighboring pixels, L_s was set to be much higher than L_p. R_s divided the bias current evenly among the pixels, and also reduced the recovery time of the array, since the time constant of the recovery time of the fired pixel was approximately $L_s/(R_s + Z_0)$.[21]

To simulate the output response from a detection event, we implemented the SNSPD electro-thermal model[22] into the array circuitry. The respective pulses from each detector firing are shown in different colors in Fig. 1(b). In the simulation, the bias in each pixel I_B was set to 16 μA and the critical current I_C was set to 20 μA. The large spacing between the peak values indicated identification would be possible even in the presence of standard electrical background noise (typically a few mV). The pixels were thus very well isolated from inter-pixel electrical crosstalk. In the simulation, a small amount of current (0.5 μA) leaked from the triggered devices into its neighbors during the output, but it was only 2.5% of I_C and was negligible in terms of its effects on device performance (see the supplementary materials[20]).

To understand the electrical behavior of the array with more elements, we analyzed $V_L - V_R$ versus the position of the triggered pixel m in an N-element current-splitting array (see the supplementary materials[20] for the derivation). The circuit architecture shows advantages that (1) the total output from each pixel is always fully diverted to the readout, minimizing the signal loss in the circuit; and (2) $V_L - V_R$ is linearly dependent on the position of the fired pixel, which is ideal for setting linearly increased thresholds for distinguishing fired pixels.

To estimate the array's tolerance of circuit element variability, we combined our electrothermal circuit model with Monte-Carlo modeling of circuit parameter variation. There

are two main possible effects that could degrade the performance of the array. One negative effect is that deviations in R_s can lead to poor bias conditions, affecting detection efficiency and output pulse levels. The other issue is that variations of L_p and L_s may result in shifts of the peaks of $V_L - V_R$ from the ideal levels.

For Monte Carlo modeling, we assumed the within-chip variability of circuit parameters was normally distributed and applied a 5% variation randomly to the resistors and 3% variation to the inductors (see the supplementary materials[20] about the experimental variation) and simulated the output again. Fig. 2 shows the simulated distribution of the traces of V_L-V_R over 780 cases of the randomly chosen circuit parameters. The pulses of each detection event can still be distinguished clearly, showing no crosstalk even between the worst cases ($>100\,mV$ separation). A quantitative discussion of the results is available in the supplementary materials[20] about the minimum spacing of the peaks of $V_L - V_R$ between pulses from neighboring pixels.

Fabrication of the array was similar to the fabrication of a single SNSPD,[23] but involved a number of extra steps to create the circuit elements and connect the pixels (see the supplementary materials[20]). The corners of the superconducting nanowires were optimized to reduce the current crowding effect.[24] We tested ~130 arrays, of which only six arrays were found to have uniform detection efficiencies among all four elements–most of the arrays only had two or three pixels working. Given the data, we have collected about the variability of the inductor and resistor circuit parameters; it is unlikely they are responsible for the low yield. More likely, some of the 80 nm detection nanowires in one or more of an array's pixels are faulty, so the yield should increase with improved lithography or advances in materials. Fig. 3 shows the images of the array. We estimated the
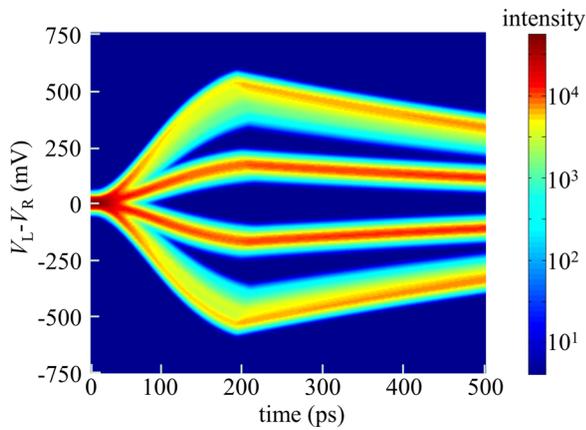
FIG. 2. Monte-Carlo electrothermal modeling of the differential signal V_L-V_R in the four-element array, including circuit variations. The pulses from top to bottom are the single-element triggering cases occurring at E_1, E_2, E_3, and E_4, respectively. The color of the pulses shows the intensity of the position where the traces appear.

nanowire inductance by counting the number of squares each wire comprised, and multiplying that by 80 pH per square of kinetic inductance.[21] The estimated inductances for L_s, L_p, and L_k were 800 nH, 52 nH, and 34 nH, respectively. The spacing between the pixels was 100 μm. The spacing of the pixels, which is the spatial resolution of the array, can be optimized for the optics that couples the light onto the array.

We measured the array in a helium-pumped cryostat with a base temperature of 1.6 K (see the supplementary materials[20] for details about the measurement setup). The pulses were captured and full digitized by a 6 GHz real-time oscilloscope to get $V_L - V_R$ which told the position information of the fired element. To better analyze the peak distributions, the high cutoff frequency was filtered to 200 MHz at the oscilloscope to remove the amplitude noise. The array performed similarly to an independent SNSPD fabricated on the same chip in terms of critical current of the nanowire, dark-count rate, and detection efficiency (see the supplementary materials[20]). To get the temporal resolution, we summed the two outputs to measure the jitter of the array. The jitters were 124 ps for the array and 70 ps for the SNSPD. Part of the increase in the jitter was caused by the large series inductor
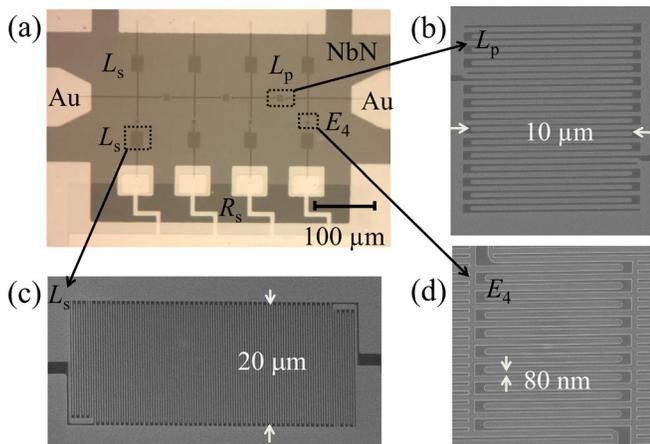

FIG. 3. Images of a four-element array. (a) Optical micrograph of the array. (b) SEM image of the current-splitting inductor L_p. (c) SEM image of the inductor L_s. (d) SEM image of an SNSPD from one of the pixels with an active area of 2.6 μm $\times$ 3.0 μm.

which slowed down the rising time of the pulse and produced additional jitter from the voltage noise.[25]

The most important characteristic of the array was that the output from each pixel was indeed distinguishable from its neighbors. In the measurement, the total bias current for the array was 66 μA, which was 0.98 of the critical current I_C (afterpulsing effects were observed when the bias current was increased above $0.98 I_C$, presumably because the pixels were connected in parallel[26]). The CW laser illuminating the array was attenuated to 9.5×10^6 photons per second. At this low photon flux, the probability of multiple pixels fired simultaneously was very low.

As seen in Fig. 4(a) of a persistence map of $V_L - V_R$, the spacing between the four pulses was above the noise floor, so the output peaks from each of the four pixels were distinguishable. Therefore, the array was virtually free of crosstalk in terms of spatial resolution, which is 100 μm, and we were able to identify the position of the triggered pixel with near-perfect accuracy by setting thresholds on the readout. We recorded the pulse heights of 15,160 pulses using the oscilloscope and plotted a histogram of the peak values of $V_L - V_R$ as shown in Fig. 4(b). Fitting each peak with a Gaussian function, the full-width-at-half-magnitude (FWHM) values of the peaks were in the range from 44 mV to 48 mV, while the spacing between neighboring peaks was 231 mV ($E_1 \sim E_2$), 248 mV ($E_2 \sim E_3$), and 268 mV ($E_3 \sim E_4$). The FWHM spreads were equal to the base noise level in our readout system, suggesting the on-chip circuit of the array did not introduce significant amounts of noise. There were a few counts that did not seem to belong to any of the four pixels, shown in magenta in Fig. 4(b). These counts are not fully understood, but were possibly caused by multi-pixel events. The array might be able to detect some of the multi-pixel events with additional signal processing. This possibility is discussed in the supplementary materials.[20]

We set thresholds for discrimination of the fired position to the middle of two adjacent peaks and counted the total number of events for each position. The number was normalized to the total number of counts from all pixels, and the distribution (ideally 25% each) came out to 25.9%, 26.0%, 22.2%, and 24.7% for pixels E_1, E_2, E_3, and E_4, respectively. The almost uniform detection shows that the four pixels were nearly identical and the array architecture did not affect photon detections.

We did a basic analysis to determine how large an array could be implemented by adding pixels to the measured array without changing the circuit or SNSPD design. From Fig. 4(b), the maximum range of the four-element array was from -384 mV to 363 mV, giving a voltage span, or operating region, of 747 mV. Using the FWHM values as the resolution level necessary to distinguish the peaks, the maximum size of the array is estimated to be $747/45 \cong 17$ pixels. The arrays could further be expanded by using existing methods, such as using parallel SNSPDs with a higher output signal,[27,28] brute-force scaling using cryogenic electronics,[29] or by using SFQ circuits to read out the differential signals.[16,17] For reading out a large array or using the array in practice, readout instruments, such as fast analog-digital converter boards with low noise, high dynamic range, and wide bandwidth, are needed.

We have demonstrated a SNSPD array with four elements which is capable of both temporal and spatial discrimination of
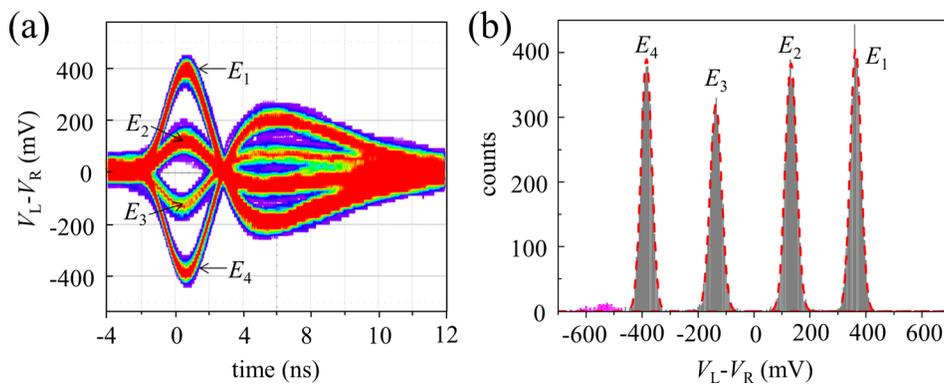
(a)

(b)

FIG. 4. Position discrimination of detection events in the four-element array. (a) Persistence map of $V_L - V_R$ captured by the oscilloscope showing pulses originating from E_1, E_2, E_3, and E_4. (b) The histogram of $V_L - V_R$ sampling for 15,160 pulses with a 5 mV bin size. Peaks are fit using Gaussian functions (dashed-red lines). The counts outside the four peaks (purple coloring) were possibly from multiple-count events.

photon arrivals. The position information was read out using a simple circuit. The positions of the triggered pixels were distinguished with negligible crosstalk for the four-element array. We modeled the array circuit using an electrothermal model for the SNSPDs and used a Monte-Carlo model to simulate variation of the circuit elements. The simulations were found to agree with our experimental results, showing that our combined model can be a useful tool for designing complex circuits with integrated SNSPDs. Based on the experimental results, we estimated that the size of the array can be increased to 17 pixels while maintaining spatial discrimination and without changing the design of the circuit. We also suggested practical ways to further increase the size of the array. Compared with the other methods, at a scale less than hundreds of pixels, our reported architecture of SNSPD-arrays based on the current-splitting method may be simpler to fabricate and read out.

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