MoS_2 Field-Effect Transistor with Sub-10-nm Channel Length

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ABSTRACT

Atomically thin molybdenum disulfide (MoS_2) is an ideal semiconductor material for field-effect transistors (FETs) with sub-10-nm channel lengths. The high effective mass and large bandgap of MoS_2 minimize direct source-drain tunneling, while its atomically-thin body maximizes the gate modulation efficiency in ultra-short-channel transistors. However, no experimental study to date has approached the sub-10-nm scale due to the multiple challenges related to nanofabrication at this length scale and the high contact resistance traditionally observed in MoS_2 transistors. Here, using the semiconducting-to-metallic phase transition of MoS_2, we demonstrate sub-10-nm channel-length transistor fabrication by directed self-assembly patterning of mono- and trilayer MoS_2. This is done in a 7.5-nm half-pitch periodic chain of transistors where semiconducting (2H) MoS_2 channel regions are seamlessly connected to metallic-phase (1T') MoS_2 access and contact regions. The resulting 7.5-nm channel-length MoS_2 FET has a low off-current of 10 pA/μm, an on/off current ratio of $>10^7$, and a subthreshold swing of 120 mV/dec. The experimental results presented in this work, combined with device transport modeling, reveal the remarkable potential of 2D MoS_2 for future sub-10 nm technology nodes.

KEYWORDS: MoS_2 FETs, sub-10 nm, phase transition, block copolymers, virtual source modeling.

As the channel length of transistors has shrunk over the years, short-channel effects have become a major limiting factor to transistor miniaturization. Current state-of-the-art silicon-based transistors at the 14-nm technology node have channel lengths around 20 nm, and several technological reasons are compromising further reductions in channel length. In addition to the inherent difficulties of high-resolution lithography, the direct source-drain tunneling is expected to become a very significant fraction of the off-state current in sub-10-nm Silicon transistors, dominating in this way the standby power. Therefore, new transistor structures that reduce the direct source-drain tunneling are needed to achieve further reductions in the transistor channel length. Transistors based on high mobility III–V materials[1, 2], nanowire field-effect transistors (FETs)[3, 4], internal gain FETs[5, 6] (such as negative capacitance devices) and Tunnel FETs[7] are among those that have been considered to date. More recently, layered 2D semiconducting crystals of transition metal dichalcogenides (TMDs), such as Molybdenum Disulfide (MoS_2) and Tungsten Diselenide (WSe_2), have also been proposed to enable aggressive miniaturization of FETs[8-11]. In addition to the reduced direct source-drain tunneling current possible in these wide-bandgap materials, the atomically thin body of these novel semiconductor materials is expected to improve the transport properties in the channel thanks to the lack of dangling bonds. Some studies have reported, for example, that single layer MoS_2 has a higher mobility than ultra-thin body silicon [12] at similar thicknesses.

Moreover, the atomically-thin body thickness of TMDs also improves the gate modulation efficiency. This can be seen in their characteristic scaling length[13] ($\lambda = \sqrt{\frac{\varepsilon_{Semi}}{\varepsilon_{ox}} t_{ox}.t_{semi}}$), which determines important short channel effects such as the drain-induced barrier lowering (DIBL) and subthreshold swing (SS). In particular, MoS_2, has low dielectric constant $\varepsilon = 4–7$[14, 15] and an atomically thin body (t_{semi} ~0.7 nm × number of layers) which facilitate the decrease of λ while its relatively high bandgap energy (1.85 eV for a monolayer) and high effective mass allow for a high on/off current ratio (I_{on}/I_{off}) via reduction of direct source–drain tunneling[16]. These features make MoS_2 in particular, and wide-bandgap 2D semiconductors in general, highly desirable for low-power sub-threshold electronics. In these applications, the on-current (I_{on}) for a given I_{off} is influenced more by the subthreshold swing (SS) than by the carrier mobility.

To demonstrate and benchmark MoS_2 transistors with channel lengths below 10 nm, two important challenges need to be overcome. First, a suitable lithography technology is required. Then, a low-contact resistance is needed for the source and drain access regions to ensure that the channel resistance will dominate the device behavior. In this work, to reduce the contact resistance we used a junction between the metallic phase of MoS_2 (1T) and its

semiconducting phase (2H) [17-19]. The atomic and electronic-band structures for the two phases are shown in Figure 1(a, b), as obtained from density functional theory (DFT). The transition from the 2H- to the 1T-phase can be triggered by exposing 2H MoS_2 to *n*-butyllithium (*n*BuLi) solution[20]. The pure 1T-phase is unstable, and undergoes a structural transition to the dynamically stable 1T'-phase[20] . Figure 1(c) compares the transfer characteristics (i.e. drain-source current vs gate-source voltage, I_{ds}-V_{gs}) of a MoS_2 FET before (2H-phase) and after (1T'-phase) phase-transition treatment of its channel layer. The metallic character of the 1T' MoS_2 channel prevents any current modulation by the gate electrode. This is in contrast to the large modulation observed for the semiconducting 2H-MoS_2 channel. Photo-luminescence (PL) spectra of monolayer 2H- and 1T' MoS_2 are shown in Figure 1 (d). The 2H-phase displays a strong PL peak at 1.85 eV originating from its bandgap, while the PL of the 1T'-phase is fully quenched because of its gapless metallicity.

The two MoS_2 phases can, in fact, coexist by forming a stable boundary between the phases[18, 20, 21]. Selective conversion of 2H MoS_2 to 1T' MoS_2 by locally masking with PMMA and exposure to *n*-butyllithium (*n*BuLi) solution was used by Kappera *et al.* [20] to demonstrate 1T' MoS_2/2H MoS_2/metal ohmic contacts with much smaller resistance than that of the 2H MoS_2/metal contacts. A variation of this technology was used in our work to form sub-10 nm 2H MoS_2 regions that act as FET channels sandwiched between adjacent 1T' MoS_2 layers that reduce the access resistance to the FET channels. This seamless 2H/1T' MoS_2 junction has a sharp atomic interface, which reduces both the physical separation between the two materials and the tunnel barrier and thus reducing the contact resistance[22, 23].

Lithography is the second challenge when realizing ultra-short channel MoS_2 transistors. Electron beam lithography can potentially provide sub-10-nm patterning resolution, however it has low throughput and it is not easy to control at these dimensions. An alternative technology is directed self-assembly (DSA) of block copolymer (BCP), which has a great potential for cost-effective, nanoscale, and high-volume manufacturing. The directionality of the features in the BCP films can be defined by physical or chemical templates created by conventional lithography [24]. A few functional devices have been fabricated to-date using BCP, including 29 nm pitch silicon FinFETs[25]. Herein, the BCP-based technique is used for the first time to pattern an MoS_2 layer in its metallic and semiconducting phases with sub-10 nm resolution.

To form the self-assembled BCP lines, two different poly(styrene-*b*-dimethylsiloxane) (PS-*b*-PDMS) BCPs were used in this work, 45.5 kg/mol (SD45; fraction of PDMS (f_{PDMS}) = 32%, period (L_0) = 43 nm) and 10.7 kg/mol

(SD10; f_{PDMS} = 25%, L_0 = 15 nm). The choice of this BCP was dictated by its high Flory-Huggins interaction parameter, as compared to other typical BCPs, such as poly(styrene-polymethyl methacrylate) (PS-PMMA). The high Flory-Huggins interaction parameter enables lower line edge roughness and a smaller period. In addition, there is a high etch selectivity between the two blocks, PS and PDMS. Using an oxygen plasma, the organic part (PS) can be easily removed while the inorganic part (PDMS) shows high resistance to etching. The key processing steps are summarized in Figure 2 (a-e). The critical step is the etching of PS regions (step 'e'). One needs to ensure that the plasma etching of PS is terminated before the MoS_2 thin films are destroyed. For this purpose, we developed an optimized etching procedure involving an initial direct oxygen plasma exposure to etch away the main portion of the PS blocks, followed by indirect plasma exposure to carefully etch the remaining PS. Details of the optimized plasma etching process are presented in Supplementary Information S4.

Figure 2 (g-m) shows SEM images of self-assembled BCP lines with pitches of 43 and 15 nm formed between Au lines that serve as end-contacts to the MoS_2 film to form the external source/drain (S/D) electrodes. The patterned MoS_2 channel was then exposed to *n*BuLi and rinsed thoroughly to selectively convert the uncovered underlying 2H MoS_2 to 1T' MoS_2, while the BCP-covered regions remained semiconducting thus forming a chain of transistors in series where each transistor is composed of a semiconducting channel and two adjacent metallic regions forming its immediate S/D contacts (see schematic in Figure 2 (f)). The length of each one of these three regions is anticipated to be equal to the half-pitch of the BCP lines which is either 7.5 or 22 nm, depending on the original pitch (15 nm vs 43 nm). The minimum number of 7.5-nm lines formed between a pair of 90-nm-spaced Au electrodes was six, while a minimum of five 22-nm lines were formed between Au lines spaced by 215 nm.

In this work, exfoliated MoS_2 flakes as well as chemical vapor deposition (CVD)-grown monolayer MoS_2 were used. The CVD technique used here is compatible with advanced device fabrication technologies and can provide full substrate coverage under optimized conditions; however CVD-grown MoS_2 currently suffers from high density of structural defects. Conversely, exfoliated MoS_2 flakes have a much lower defect density but are very small in size; only tens of micrometers in diameter. MoS_2 flakes also allow the fabrication of transistors with few-layer-thick MoS_2 channels, which can potentially stand the damage induced by plasma treatment better than monolayer CVD MoS_2 because only the topmost layer is affected by plasma treatment. Here we focus on the experimental performance of a device with 7.5-nm channel length constructed on exfoliated trilayer MoS_2, which exhibits the best performance and shortest channel length among the fabricated devices. Details of CVD monolayer

devices with 7.5- and 22-nm channel lengths are provided in the Supplementary Information S5. In all studied devices, highly doped Si substrates with a 10 nm of HfO_2 layer on the surface are used as the back-gate stacks. The device fabrication process is described in detail in part S3 of the Supplementary Information. Figure 3 shows I_{ds}-V_{gs} and I_{ds}-V_{ds} characteristics of a trilayer MoS_2 FET at different processing steps. As shown in Figures 3(a) and (b), the as-fabricated device with channel length of 90 nm shows good subthreshold characteristics with small DIBL< 0.1V/V, SS = 88 mV/dec and current saturation in I_{ds} -V_{ds} characteristics owing to velocity saturation.

The chain of in-series 7.5-nm MoS_2 FETs, formed after the *n*BuLi treatment, shows a well-defined I_{ds}-V_{gs} performance with an I_{on}/I_{off} ratio in excess of 10^7 with SS_{min} of 120 mV/dec and I_{on} of 0.25 mA/μA at V_{ds} = 1 V (Figure 3(d)). These characteristics are further explored using device modeling in the discussion that follows. Thanks to the extremely thin body thickness and the wide bandgap of the MoS_2 channel, the short channel length of this device has a minimum impact on its subthreshold characteristics and the off-state current, I_{off} < 10 pA/μm. However, compared with the I_{ds}-V_{gs} characteristics of the long channel (Figure 3(a)), the device shows larger DIBL of ~ 0.7 V/V. This also leads to the absence of saturation in the I_{ds}-V_{ds} curves (Figure 3 (e)) despite the high current density in the mA/μm range, which is rather high for MoS_2 transistors.

To further analyze the performance of the sub-10-nm MoS_2 channels, we used the MIT Virtual Source Compact model (MVS)[26] to fit the experimental data for the MoS_2 FETs. In the past, the MVS model has been applied to short channel silicon[26], III-V semiconductors[27-29] and graphene[30] to extract device parameters such as injection velocity, carrier mobility, and access resistance (which is equivalent to the 2H/1T' junction resistance in this work). Here, gate capacitance, channel length, DIBL and subthreshold swing are directly determined from the experimental data while the remaining parameters (carrier mobility and velocity) are extracted by best-fitting the full I-V data. In addition to the chain of MVS-model-standard 2H/1T' FETs in series, we also model the non-linear gate voltage-dependent Au-MoS_2 contact resistance (R_s and R_d) at the external source and drain regions as two additional transistors in series with the chain of transistors. Figure 4(a, b) compares the experimental transfer and output characteristics of the trilayer MoS_2 chain of in-series FETs with the model fitting. The parameters of the contact-modeling transistors were used purely as fitting parameters here; however, we found that the resulting contact resistance and its gate voltage dependence are well matched with the experimental Au-MoS_2 contact resistance data extracted in this work (Supplementary Information S6). The injection velocity (v_{xo}) and the mobility are found to be ~1×10^6 cm/s and 25 $cm^2/V\cdot s$, respectively. This mobility is the Matthiessen combination of diffusive and ballistic

mobility, which gives the mean free path to be around 2.1 nm. The access resistance (where $r_s = r_d = r_{2H/1T'}$) is as low as 75 Ω·μm, which indicates the ohmic nature of the 2H/1T' junction; this aspect will be further discussed later in this work. The device also has a very low I_{off} (<10 pA/μm) and high I_{on}/I_{off} ratio, in good agreement with previous theoretical expectations[31, 32]. This is a result of the ability of MoS_2 to suppress direct source-drain tunneling thanks to its high effective mass.

The lack of saturation in the I_{ds}-V_{ds} characteristics and the deviation of the current from the MVS model (for V_{ds} > 0.6 V) as indicated in Figure 4(b), is mainly because of large DIBL induced by the relatively large effective oxide thickness (EOT) used in this work (~4 nm, vs ~0.8 nm in state-of-the-art CMOS technology). To clarify this point, we performed quantum mechanical simulations using non-equilibrium Green's function (NEGF) formalism for a single 7.5-nm MoS_2 FET. For the thicker oxide (4-nm EOT, Figure 4(c)), the barrier at the off-state (V_{gs}=0) with high drain bias (V_{ds}=0.6 V) is low enough to cause both high thermal emission currents and direct source-drain tunneling. This is in good agreement with the experiments (Figure 4f), however it should be noted that as the experimental device has six transistors in series, it takes roughly six times the voltage drop across one transistor to produce the same level of tunneling current predicted by the simulation. It should be noted that for low V_{ds} values (up to ~0.6 V), the tunneling contribution is negligible (less than 10%) and the transport is determined by thermal emission.

NEGF simulations of a thinner oxide (0.75-nm EOT) predict a significant reduction in the transmission probability of at least five orders of magnitude both below and above the barrier (Figure 4(d)). This is because the barrier height is now higher and the potential reaches the peak much more quickly thanks to the lower scaling length. The effective mass of MoS_2 is large enough to reduce DIBL for the 0.75-nm EOT to approximately 72 mV/V and the subthreshold slope to about 73 mV/dec, as shown in Figure 4(e).

Figure 4(g) and (h) show the MVS-calculated transfer and output characteristics of a single 7.5-nm MoS_2 transistor, as modeled using the DIBL and subthreshold slope parameters extracted from the NEGF simulation with a 0.75-nm EOT and Vt=0.5 V (Figure 4(e)). In these simulations, the velocity, mobility and resistance ($r_{2H/1T'}$=75 Ω·μm) were taken from the MVS fit of the trilayer device. The device shows an I_{on}/I_{off} in excess of 10^6 with I_{off} as low as ~100 pA/μm and I_{on} of ~230 μA/μm at $\underline{V}_{gs}$=0.6 V. These numbers are not far from the requirements envisaged in the International Technology Roadmap for Semiconductors (ITRS)[33] for the 2024 low-power devices node (L_g = 7.5 nm, I_{on} = 400 μA/μm, I_{off} = 10 pA/μm). Further improvements in both the contact resistance and the

on current are required however, which may be made possible by the development of better MoS_2 growth techniques.

Finally, we would like to highlight two important points about the 2H/1T' junction that must be addressed. The first is the stability of the 1T' phase and the stability of its junction with the 2H phase, and the second is the formation of an ohmic interface, *i.e.*, a low barrier contact between the two phases that allows the 1T' regions to act as suitable source or drain contacts to the 2H MoS_2 channel. Because MoS_2 FETs are *n*-type, these contacts must have a low work function to form effective ohmic contacts. To determine whether or not the 2H/1T' MoS_2 junctions fulfill these requirements, we performed DFT calculations of the 2H MoS_2 phase and of both pristine and functionalized 1T' phases and their junctions. The pristine 1T' phase has a high work function of 5.8 eV when compared with the electron affinity of 2H MoS_2, which is ~4.3 eV as shown in Figure 5(a) and (b). Such a large energy difference would form a significantly high Schottky barrier for both MoS_2 thicknesses and would impede the formation of an ohmic contact. However, as shown by the experimental results, $r_{2H/1T'}$ is relatively small (~75 $\Omega \cdot \mu m$), thus demonstrating the ohmic nature of the 2H/1T' junction. To understand this apparent contradiction, we must assess the effects of surface adsorbates or functional groups in changing the charge density and thus the work function of 1T' MoS_2. In fact, the adsorption of chemical species on the surface of 2D materials is known to modify their electronic properties. Given the chemical phase transition treatment that is applied in this work, which involves the formation of a lithium molybdenum sulfide (Li_xMoS_2) intermediate compound that requires a hydration reaction to remove the lithium content, the most probable adsorbates are hydrogen (H) functional groups[17]. Therefore, we used DFT calculations to study the properties of H-doped 1T' MoS_2, where the H atoms are bonded to the sulfur atoms, which is the most favorable configuration. The results showed that H adsorption leads to further structural stabilization of the 1T' phase. The pristine 1T' phase is less stable than the 2H phase by 0.55 eV per MoS_2 molecule, but it becomes more stable by 0.16 eV per MoS_2 molecule with full H coverage of 0.5/Mo. We then constructed an atomic model and performed a structural relaxation analysis of the 2H/1T' MoS_2 junction with H adsorbed on the 1T' region only. The results showed that each phase remained stable after optimization and formed a stable boundary, which is in good agreement with the results of previous direct observations of 1T' and 2H phases in coexistence[20]. The relaxed atomic structure of their boundary are shown in 5 (c). We note that a recent theoretical work[34] reported the structural stability and electronic properties of a similar structure between the S-edge 2H MoS2 and 1T' MoS_2. Here, we observed that H adsorption raises the Fermi level and therefore substantially reduces the

work function of 1T' MoS_2 to about 4.4 eV at 0.5 H/Mo coverage, which eases ohmic contact formation by significantly reducing the energy barriers; this may also explain the small resistance observed in the 2H/1T' junction. More details about the effects of H adsorption as well as other functional groups, *e.g.* oxygen and hydroxyl (-OH) groups, on the stability and electronic structure of the 1T' phase are presented in the Supplementary Information S7. We also calculated the partial charge densities at the boundaries between 2H MoS_2 and H-functionalized 1T' MoS_2 as shown in Figure 5(e). The calculations show that the electronic states closest to the Fermi level are not only from the metallic 1T' phase, but also contain a substantial contribution from the atoms closest to the boundary in the semiconducting 2H phase. This lateral orbital overlapping, which stemmed from the seamless 2H/1T' interface, further guarantees the ease of electron transition across the 2H/1T' side-contact.

In summary, we have demonstrated the smallest MoS_2 transistor fabricated to date by aggressive channel length scaling to the sub-10-nm regime using DSA patterning of mono- and trilayer MoS_2 in a periodic chain of junction semiconducting (2H) and metallic-phase (1T') MoS_2 regions with a half-pitch of 7.5 nm. The MoS_2 composite FET had an I_{off} of 10 pA/μm and an I_{on}/I_{off} in excess of 10^7. Modeling of the device current-voltage characteristics revealed that the 2H/1T' MoS_2 junction has record-low resistance of 75 Ω·μm, while trilayer 2H-MoS_2 exhibits a low-field mobility of ~25 $cm^2/V{\cdot}s$ and a carrier injection velocity of ~10^6 cm/s. DFT calculations of the 2H/1T' junction further confirmed the stability of the interface and indicated its ohmic nature. These results highlight the great promise of MoS_2 transistors fabricated at the limit of the ITRS technology roadmap.

Methods:

Dry transfer of MoS_2 flakes:
Few-layer MoS_2 devices were prepared by the commonly used pickup and dry transfer methods [35, 36]. MoS_2 was mechanically exfoliated to obtain few-layer isolated flakes from commercially available bulk MoS_2 crystals on pre-cleaned (*i.e.*, Piranha solution, oxygen plasma and solvent) substrates. A polydimethylsiloxane (PDMS) sheet was cut into small pieces and placed on a pre-cleaned glass slide with double-sided tape. A 6% solution of polypropylene carbonate (PPC, Sigma Aldrich) in chloroform was then spin coated on the glass/tape/PDMS stack. This transfer slide was loaded into the probe arm of the transfer setup and brought into contact with the desired flake at room temperature. The stage was heated to 90 °C and maintained at that temperature for 1 min. After the temperature of the stage was returned to room temperature, by natural or forced cooling, the transfer slide was slowly disengaged. The picked-up flake was transferred to the pre-patterned via holes and heated to 155 °C to release the polymer. The polymer was dissolved in chloroform, and the structure was cleaned with solvent and annealed (200 sccm Ar/200 sccm H_2) at 360 °C for 3 hours.

Phase Transformation of MoS_2:
To achieve phase transformation in MoS_2, we used a common chemical method[20, 37] involving exposure of 2H-MoS_2 to *n*BuLi solution, which is a strong reducing agent. 2H-MoS_2 samples were immersed in 2M *n*BuLi (10 mL, Sigma Aldrich) in a N_2-filled glovebox and then rinsed thoroughly with hexane. Li atoms can be inserted into MoS_2 layers to form Li_xMoS_2, the hydration of which results in MoS_2 and LiOH.

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AUTHOR CONTRIBUTIONS

A.N. conceived the device, coordinated the study and performed the device measurements. A.Z. fabricated the MoS_2 devices, performed the optical characterizations and contributed to the device measurements. R.S. designed the

device modeling approach and performed the modeling. A.T. developed DSA-BCP technique and applied it to the MoS_2 devices. X.L. grew CVD MoS_2. W.C. and S.F. performed the DFT calculations. M.D., J.K., E.K., K.B., D.A. and T.P. supervised the research and provided scientific support. All authors contributed to the writing of the manuscript.

Supporting Information:

The Supporting Information is available free of charge on the ACS Publications website at DOI:

Additional data concerning: CVD growth and Raman characterization of MoS_2, device fabrication, Block copolymer self-assembly and details of MVS, NEGF and DFT calculations.

FIGURES:

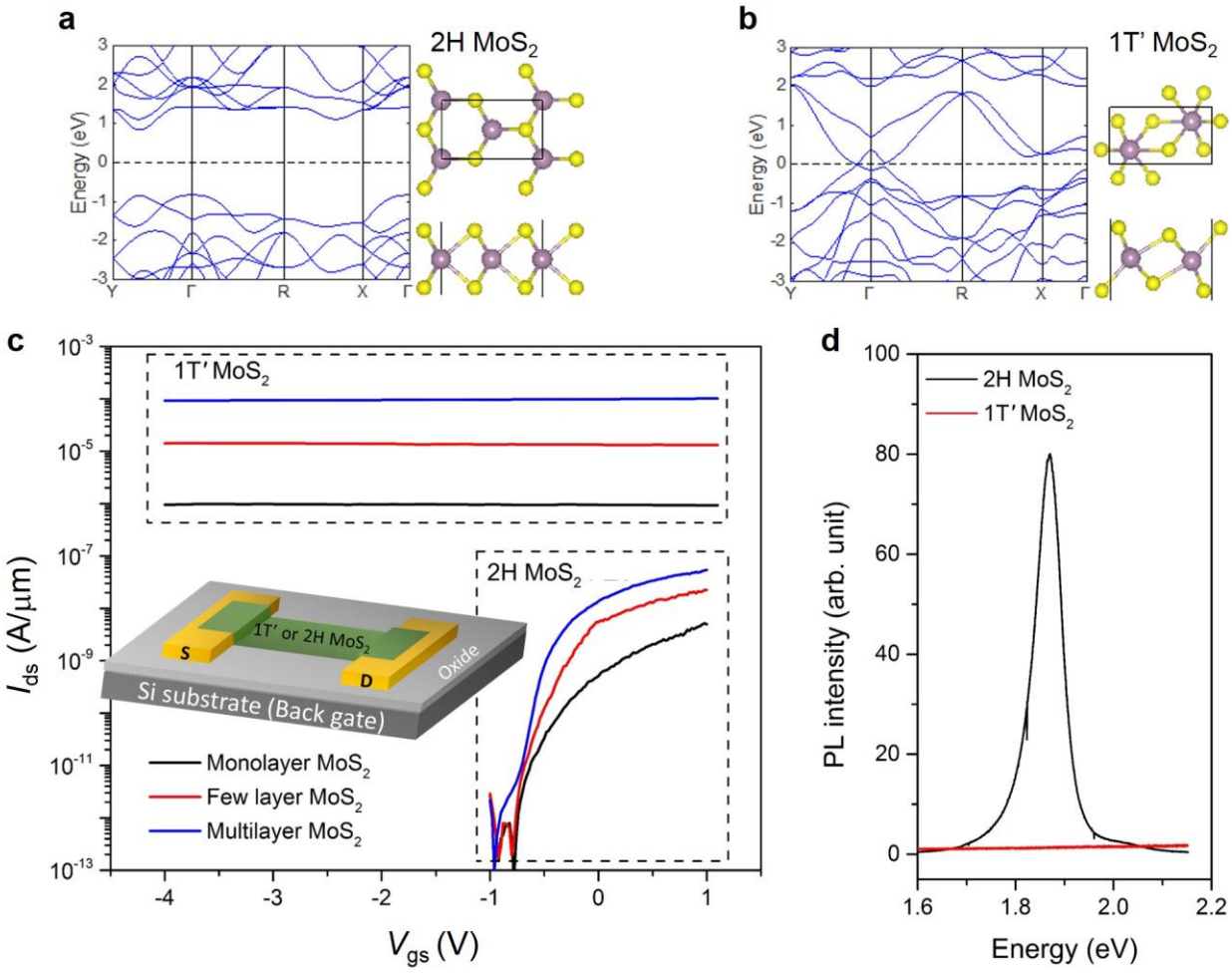

Figure 1. (a ,b) Electronic band structures of 2H and 1T' MoS_2 and their atomic structures. The 2H band structure shows a bandgap of approximately 1.8 eV, while the conduction and valance bands of 1T' MoS_2 are overlapped; therefore, 1T' MoS_2 has metallic gapless characteristics. (c) Transfer characteristics of three MoS_2 FETs with different thicknesses of MoS_2 before and after phase transition treatment . The intrinsic 2H MoS_2 FETs show strong semiconducting behavior with large gate modulation, while all of them after the phase transition show constant current, increasing with thickness, with almost no gate modulation featuring metallic 1T' MoS_2. (d) PL spectra of monolayer 2H and 1T' MoS_2. The 2H phase shows a strong PL peak at 1.85 eV generated by its bandgap, while the PL of the 1T' phase is completely quenched owing to its gapless metallic characteristics. See Supplementary Information S1 and S2 for CVD growth of monolayer MoS_2 and Raman characteristics of different phases of MoS_2, respectively.

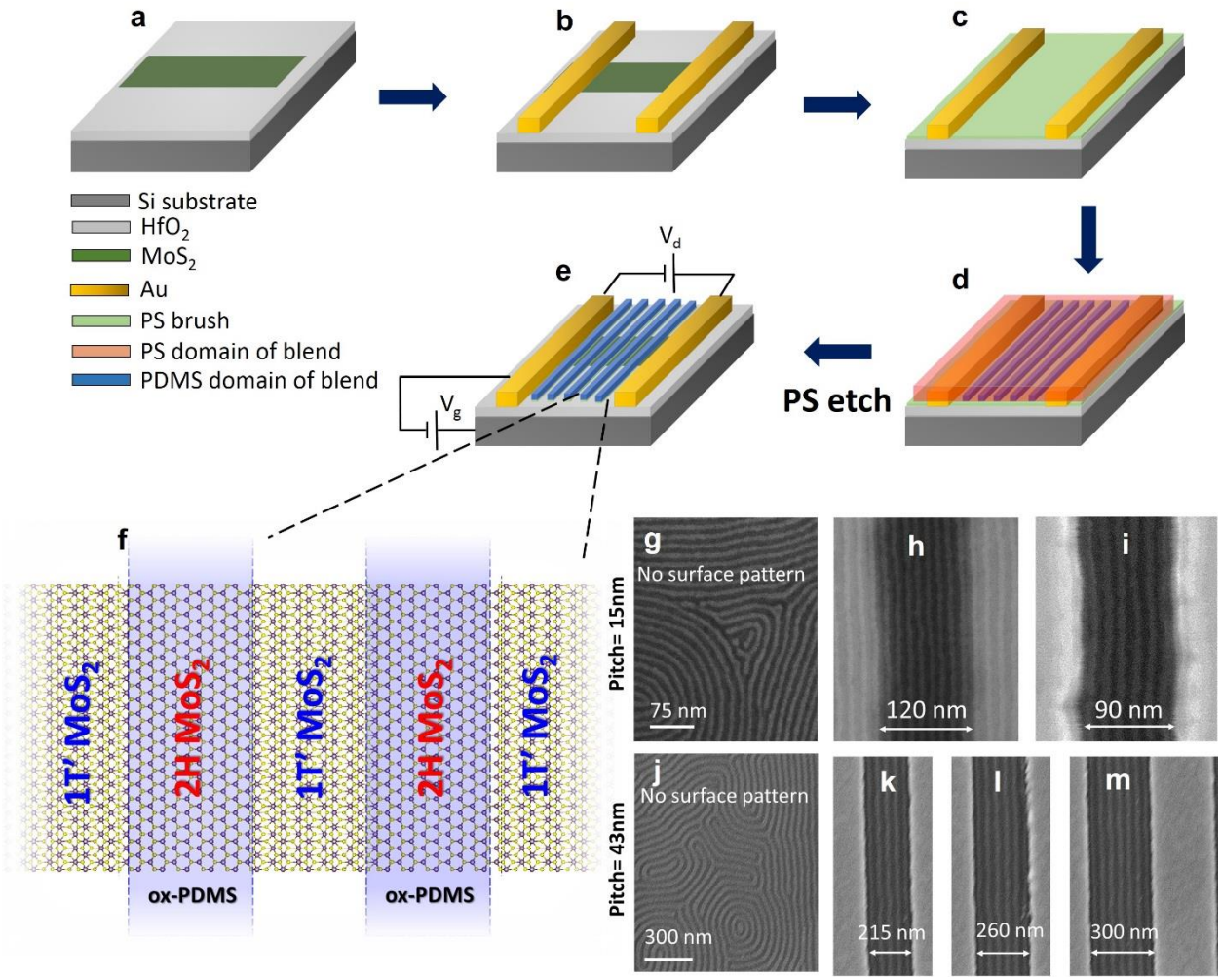

Figure 2. (a) The deposition of MoS_2 on a HfO_2-coated Si wafer (see Supplementary Information S3, for details of substrate preparation) is followed by (b) Au metallization by e-beam lithography to form contacts to MoS_2. These contacts are used as the S/D electrode in the long channel MoS_2 FET (before phase transition treatment) and as the end-contacts for the chain of 2H/1T' MoS_2 FETs (after the phase transition). Next, (c) MoS_2 is functionalized with a PS brush and then (d) spun PS-*b*-PDMS BCP followed by an annealing step that leads to microphase separation of the blocks and finally (e) selective etching of the PS and leave ox-PDMS patterns on the substrate. After that (not shown here; see Supplementary Information S4 for details) the sample will be treated with nBuLi for 2H to 1T' phase transition in the non-protected regions. Panel (e) also shows the biasing schematic of the MoS_2 chain FETs, where the Si substrate is used as the back-gate and the Au electrodes are used as end contacts; and (f) shows a schematic of the patterning in the 1T' and 2H MoS_2 sequencing regions. SEM images show PDMS lines with (g–i) 15 nm and (j–m) 43-nm pitches after PS etching on surfaces with no guide pattern as well as surfaces with Au lines with different

spacings to act as guides. The absence of a guide pattern leads to random formations of the PDMS lines while in patterned surface lines are self-assembled (in parallel) with the Au electrodes.

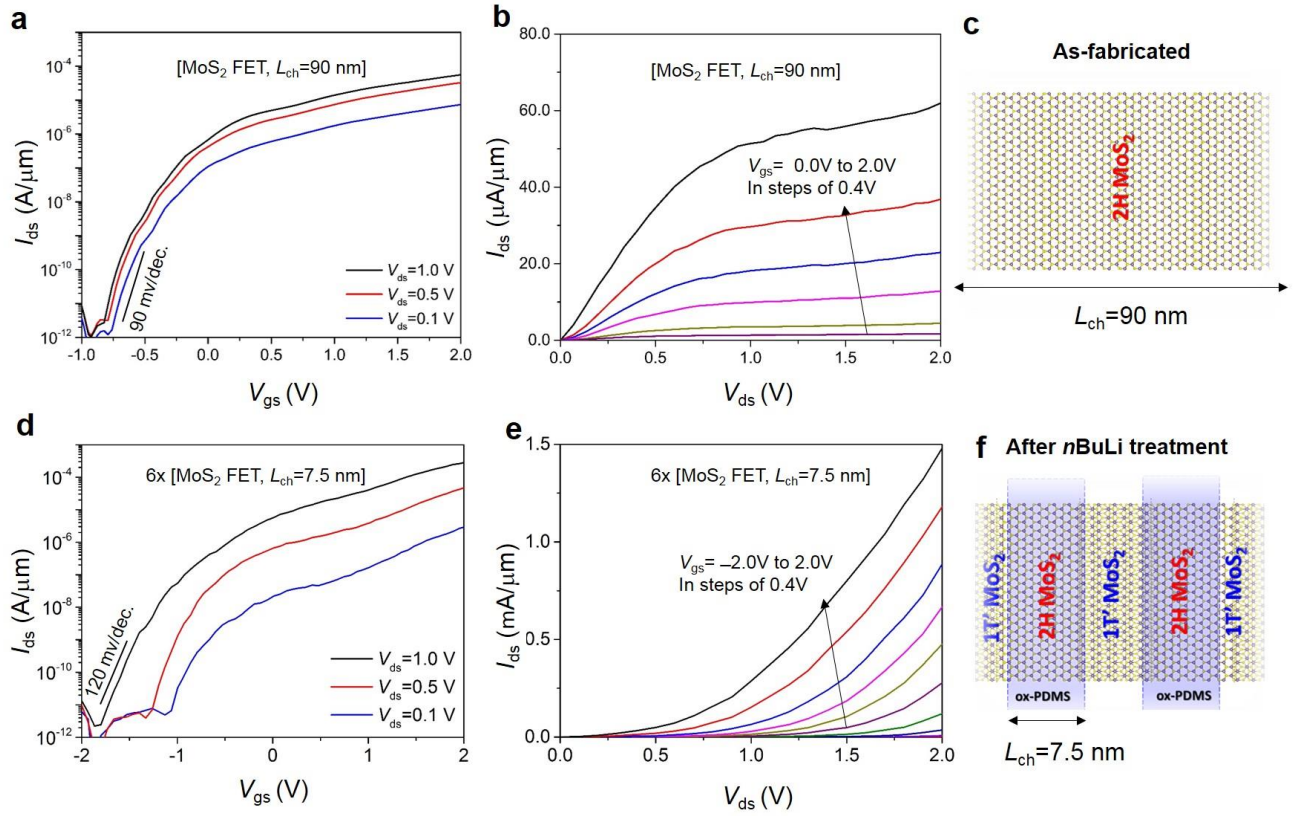

Figure 3. (a) and (b) I_{ds}–V_{gs} and I_{ds}–V_{ds} of an as-fabricated trilayer MoS_2 FET with channel length of 90 nm and EOT of 4 nm. (c) shows schematic of 2H MoS_2 channel. (d) and (e) The same set of *I-V* curves for the chain of six 7.5-nm MoS_2 in-series FETs produced after a phase transition treatment with *n*BuLi. The device demonstrates an I_{on}/I_{off} of ~ 10^7, low I_{off} of ~ 10 pA/μm and a subthreshold slope of 120 mV/dec for more than two decades. The transfer characteristics in (d) exhibits a DIBL of 0.7V/V which results in the lack of saturation in the drain current in (e). As discussed in the modeling section, this DIBL can be significantly suppressed by solely decreasing the EOT and thus enhancing the electrostatic control with the gate. (f) shows schematic of alternating 2H/1T' MoS_2 regions.

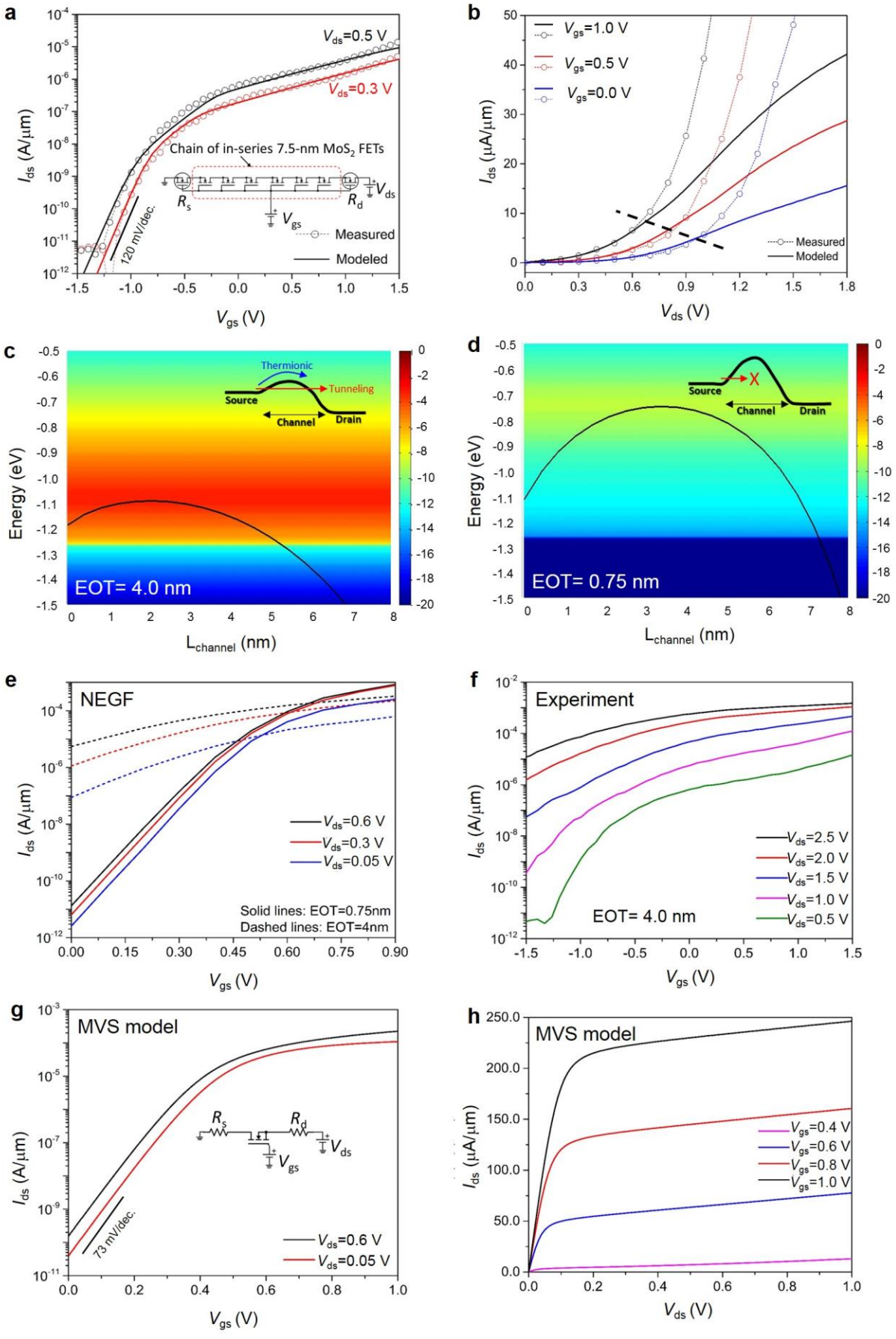
a
V_{ds}=0.5 V
V_{ds}=0.3 V
Chain of in-series 7.5-nm MoS_2 FETs
R_s
R_d
V_{ds}
V_{gs}
120 mV/dec.
Measured
Modeled
I_{ds} (A/μm)
V_{gs} (V)
b
V_{gs}=1.0 V
V_{gs}=0.5 V
V_{gs}=0.0 V
Measured
Modeled
I_{ds} (μA/μm)
V_{ds} (V)
c
Thermionic
Tunneling
Source
Channel
Drain
EOT= 4.0 nm
Energy (eV)
$L_{channel}$ (nm)
d
Source
X
Channel
Drain
EOT= 0.75 nm
Energy (eV)
$L_{channel}$ (nm)
e
NEGF
V_{ds}=0.6 V
V_{ds}=0.3 V
V_{ds}=0.05 V
Solid lines: EOT=0.75nm
Dashed lines: EOT=4nm
I_{ds} (A/μm)
V_{gs} (V)
f
Experiment
V_{ds}=2.5 V
V_{ds}=2.0 V
V_{ds}=1.5 V
V_{ds}=1.0 V
V_{ds}=0.5 V
EOT= 4.0 nm
I_{ds} (A/μm)
V_{gs} (V)
g
MVS model
R_s
R_d
V_{ds}
V_{gs}
73 mV/dec.
V_{ds}=0.6 V
V_{ds}=0.05 V
I_{ds} (A/μm)
V_{gs} (V)
h
MVS model
V_{gs}=0.4 V
V_{gs}=0.6 V
V_{gs}=0.8 V
V_{gs}=1.0 V
I_{ds} (μA/μm)
V_{ds} (V)

Figure 4. (a) and (b) MVS fit of the transfer and output characteristics. I_{ds}–V_{ds} fits the model well for V_{ds} <0.6 V. At higher voltages, the direct source-to-drain tunneling becomes substantial. The dashed line in (b) is intended as a visual guide to indicate the two regimes. The inset in (a) shows the circuit configuration used in the MVS model consisting of a chain of six 7.5 nm MoS_2 FETs and V_{gs}-dependent R_s and R_d. (c) Energy-resolved total transmission probability T (scale is in $\log_{10}(T)$ and T is in units of nm^{-1}) from NEGF simulation for EOT of 4 nm, showing substantial tunneling through the barrier in the off state with high drain bias of V_{ds} = 0.6 V. (d) T for EOT of 0.75 nm, where the tunneling current this time is suppressed by orders of magnitude. Insets in (c) and (d) schematically illustrate the tunneling and thermal emission currents (e) transfer characteristics from NEGF for two different EOTs, showing significantly improved subthreshold slope and DIBL for the EOT of 0.75 nm. (f) Experimental I_{ds}-V_{gs} curves of the chain of 7.5-nm MoS_2 FETs at different values of V_{ds} showing substantial increase of I_{off} with increasing V_{ds}, in agreement with the modeling in (e). (g) and (h) MVS prediction of transfer and output characteristics, taking into account the mobility, injection velocity and resistance found in (a),(b). EOT of 0.75 nm is used. DIBL (72 mV/V) and subthreshold slope (~73 mV/dec.) are taken from (e). See Supplementary Information S6 for details of the MVS and NEGF models.

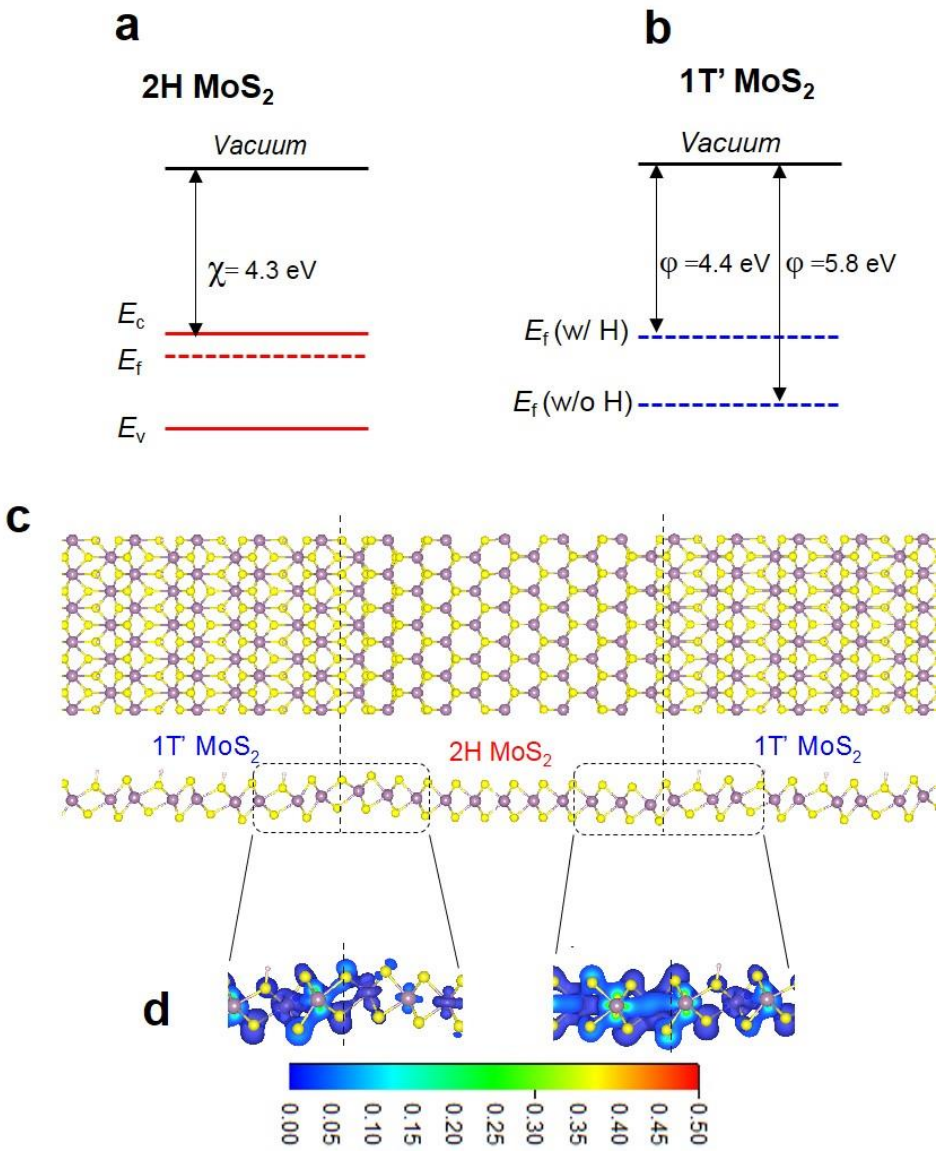

Figure 5. (a) Band diagram of 2H MoS_2. The calculated electron affinity value is χ= 4.3 eV. (b) Calculated work function (φ) values of 1T' MoS_2 with and without the H functional groups. (c) Calculated atomic structure of 2H/1T' MoS_2 boundary with H adsorbed on the 1T'-phase. To reduce the computational cost, we modeled alternating ~3-nm-long 1T'-phase and ~3-nm-long 2H-phase layers. (d) Contour plots of partial charge densities associated with the states in the energy range of [E_F−1.0 eV, E_F] at the two boundaries between the 1T'- and 2H-phases. The numbers in the color bar are in units of e/Å^3. The isosurface levels are selected at 0.02 e/Å^3. The partial charge density distribution on the side of the 1T' phase is very similar at the two boundaries (see Figure S14 for the entire device); while on the 2H-phase side, the different edge (Mo-edge and S-edge) termination results in distinctly different density distributions. See Supplementary Information S7 for details of DFT calculations.

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Supplementary Information

MoS_2 Field-Effect Transistor with Sub-10-nm Channel Length

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CVD growth of MoS_2

MoS_2 monolayers were fabricated by chemical vapor deposition (CVD) using the seed-promoted method[1]. In our synthesis (Figure S1(a)), the precursors, molybdenum trioxide (MoO_3) and sulfur (S), were loaded in two crucibles separated in the quartz tube. A 300 nm SiO_2/Si substrate was placed face-down on the crucible loaded with MoO_3. The seeding promoter, perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS), was applied on the substrate surface. Before heating, the whole CVD system was purged with 1000 sccm Ar (99.999% purity) for 3 min. Then, 5 sccm Ar was introduced into the system as a carrier gas. The system was heated to 650 °C at a rate of 15 °C /min, and MoS_2 was synthesized at 650 °C for 3 min under atmospheric pressure. The temperature at the position where the sulfur was located was set to be around 180 ^{0}C during growth. The system was finally cooled down to room temperature quickly by opening the furnace and taking out the quartz tube, and 1000 sccm Ar flow was used to remove the reactants. With the assistance of the seeding promoter, continuous monolayer MoS_2 film with triangle domain shapes were synthesized on the substrate. Figure S1 (b) shows SiO_2/Si substrates with different coverages of MoS_2 ranging from isolated triangular single crystal MoS_2 to full coverage.

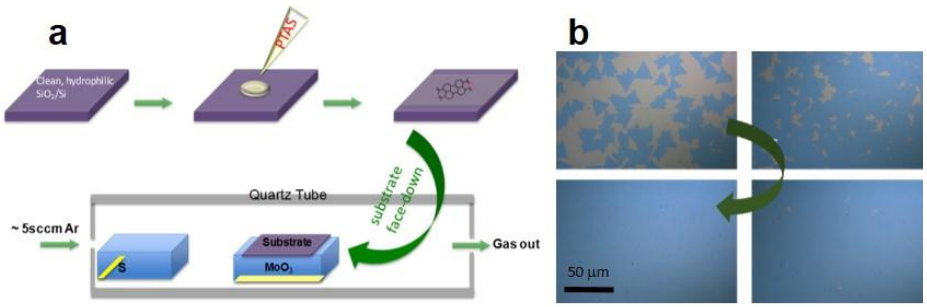

Figure S1. (a) Schematic illustration of CVD setup for monolayer MoS_2 growth. (b) Optical images of monolayer MoS_2 films on SiO_2/Si substrate at different coverage stages.

Raman Characterization of MoS_2

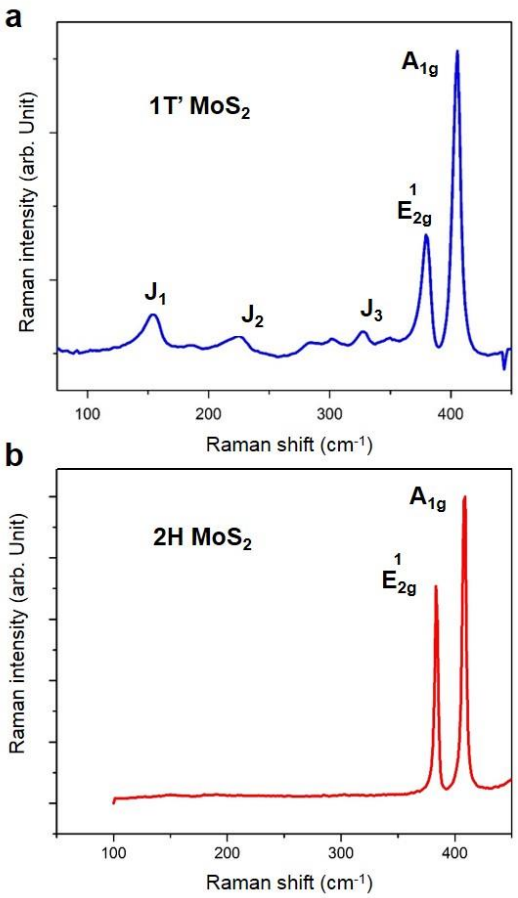

Figure S2. Raman spectra of (a) Few-layer 1T' MoS_2 and (b) Few layer 2H MoS_2.

The Raman spectra of MoS_2 samples were measured using a Raman spectrometer (Horiba LabRAM) with a 532-nm laser with a beam spot size of ~1 µm. Figure S2 compares the Raman spectra of 1T' and 2H MoS_2. The 2H-phase of MoS_2 exhibits two distinct Raman modes, E_{2g} at 385 cm^{-1} and A_{1g} at 405 cm^{-1}, while the 1T' MoS_2 shows additional peaks that arise from the distorted octahedral crystal structure[2]. These additional peaks are commonly known as J_1, J_2 and J_3, which are located at around 155, 225 and 335 cm^{-1}, respectively[2-4]. The presence of these three peaks confirms the phase transformation of 2H MoS_2 into 1T' MoS_2.

Device fabrication:

Typically, heavily doped Si substrates coated with ~300 nm of SiO_2 are used as the back-gate stack in 2D FETs. The reasons for using such a thick oxide layer are twofold: to obtain sufficient optical contrast to locate micrometre-wide flakes, and to avoid large gate leakage, because the Si substrate is a global back gate with 100% overlap with the source/drain contacts and measurement pads.

To enhance the performance of the transistors and improve gate efficiency, we need to increase the gate dielectric capacitance whilst keeping the gate leakage current as low as possible. Herein, a simple solution is used to solve this problem: we fabricate the transistor channel on a thin high-k dielectric, for example, HfO_2, while the metal pads and wires are isolated using the thick SiO_2 layer (Figure S3). In this configuration, the transistor benefits from a global back gate that provides low contact resistance, and the gate leakage current is also reasonably low.

For the scaled gate dielectric devices, 30 × 30 µm via holes were defined on a 90-nm SiO_2/Si substrate by electron-beam lithography. These via holes were then wet etched followed by atomic layer deposition of 10 nm of HfO_2 using tetrakis(dimethylamido)-hafnium (IV) and water at 250 °C. The sample was annealed in forming gas at 400 °C to reduce the bulk oxide traps. The subsequent lithography steps were the same as those used for regular devices.

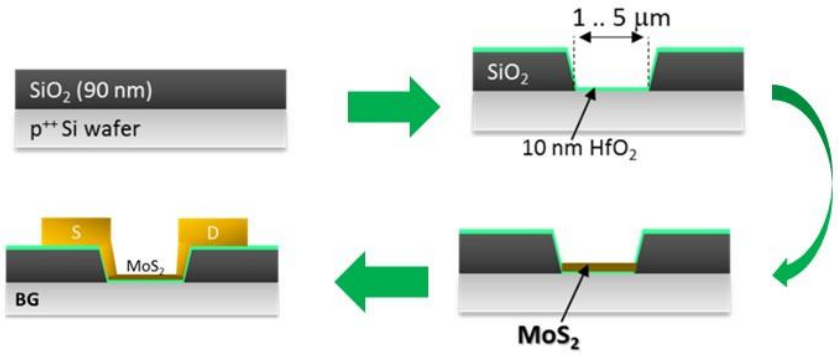

Figure S3. Schematic illustration of back-gated MoS_2 FET fabrication in SiO_2 via holes with a thin dielectric layer (10 nm of HfO_2).

Block copolymer Self-assembly

First, regular MoS_2 FETs were fabricated on highly doped Si wafers coated with 10 nm of HfO_2 as the back gate stack and contacting with gold electrodes using electron-beam lithography as source/drain contacts. Next, hydroxyl-terminated polystyrene brush (PS-OH; 1.2 kg/mol, Polymer Source) was used to functionalize the surface of the substrates. PS-OH in propylene glycol monomethyl ether acetate (PGMEA) was first spin-coated on the substrate surface, which was then thermally annealed in a vacuum oven at 170 °C for 15 h, and subsequently rinsed with toluene. Next, a monolayer of PS-*b*-PDMS BCPs was spin-coated on the surface of the substrate. Two different PS-*b*-PDMS BCPs were used in the experiments: 45.5 kg/mol (SD45; fraction of PDMS (f_{PDMS})=32%, period (L_0)=43 nm) and 10.7 kg/mol (SD10; f_{PDMS}=25%, L_0=15 nm). Then, 2 wt% SD45 was dissolved in PGMEA and 0.7 wt% SD10 was dissolved in cyclohexane for spin coating. The monolayer thicknesses of the BCPs were 29 nm for SD45 and 22 nm for SD10, and were determined by spin-coating speed. Solvent vapor annealing was performed at room temperature in a capped glass beaker. Toluene and acetone vapor was used for SD45 and SD10, respectively. This resulted in swelling of PS-*b*-PDMS BCPs, which promoted the microphase separation of the blocks. The annealing process formed periodic in-plane PDMS cylinders in the PS matrix parallel to the gold lines. Finally, CF_4 reactive ion etching was used to remove the top PDMS wetting layer followed by oxygen plasma removal of the PS matrix to leave the oxidized PDMS (ox-PDMS) patterns on the surface of the substrates parallel to the gold lines. To avoid etching of the underlying MoS_2 layer and to minimize the effect of plasma treatment on its structure, the oxygen plasma step was carried out in two parts involving direct plasma exposure for 9 s followed by placing the sample on a glass coverslip and holding it upside down 1 cm above the chuck (Figure S4). Finally, we ran a sequence of plasma

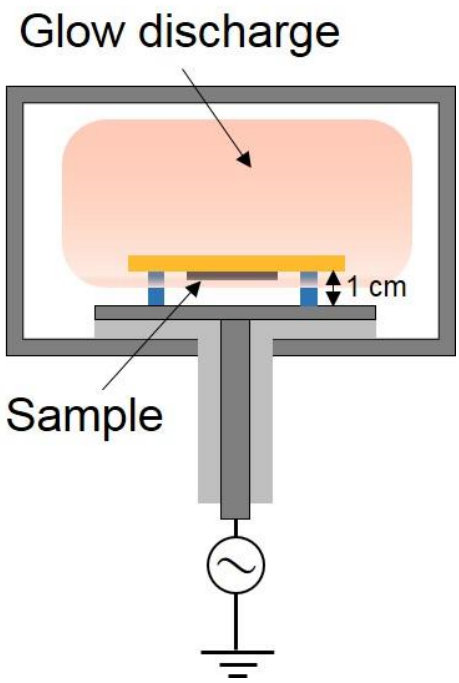

Figure S4. Plasma setup and sample configuration used in indirect plasma PS-etching.

pulses where the plasma power was ramped from 0 to 50 W in 3 s. This indirect plasma exposure helps to markedly lower the physical effect of the oxygen radicals and to limit their reaction with the target, thus providing fine etching of PS with minimum damage to MoS_2. However, mild functionalization of the topmost layer of MoS_2 with oxygen groups still occurred.

In this work, the goal was to decrease the number of transistors in series by making smaller Au gaps and thus fewer PDMS lines, which define the FET channel. The metal lift-off process used here allowed us to decrease the gap to 50 nm, which can potentially provide three FETs in series. However, we observed that when the gap was below 80 nm, the orientation of the PDMS lines changed from parallel to the Au contacts to perpendicular, as shown in Figure S5(a). This result is similar to the results of our previous work[5]. Through experiments and simulations, we showed that for small gaps, when the walls of the gaps are weakly attractive to both the PS and PDMS blocks, the PDMS lines will be formed orthogonal to the walls.

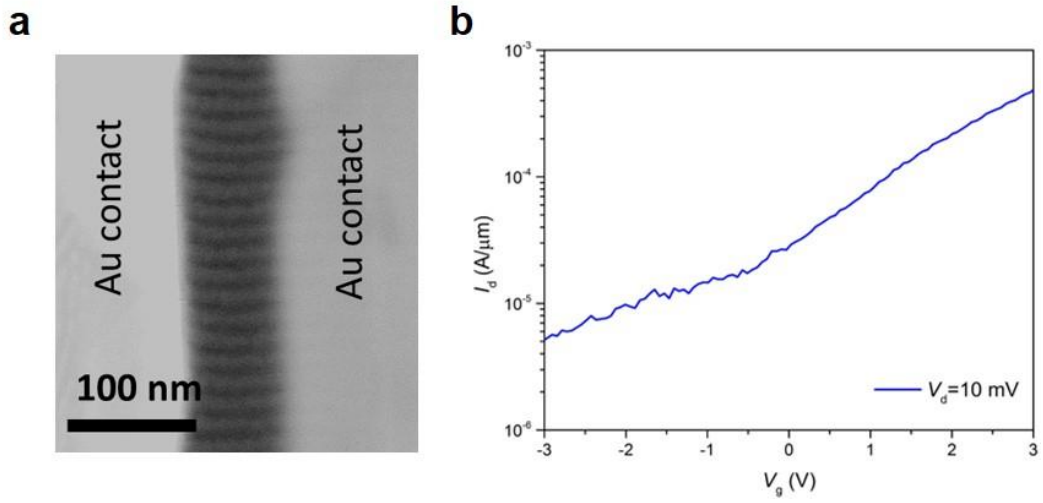

Figure S5. (a) SEM images of a MoS_2 FET with a 60-nm gap between to its Au end contacts patterned with ox-PDMS lines showing a perpendicular configuration. (b) I_{ds}-V_{gs} curve of the device showing weak gate modulation of the current, confirming that the end contacts are shorted by the perpendicular metallic 1T'-MoS_2 regions.

Therefore, the BCP self-assembly method maintains the pattern density of the lithography process. Depending on the molecular weight of the BCP and the gap between the Au lines, the number of ox-PDMS cylinders appearing between the lines varies. When the PDMS lines are perpendicular, the Au end contacts are always shorted after the MoS_2 in the gaps between them undergo a 2H to 1T' phase transition. This is confirmed by the I_{ds}-V_{gs} measurement of the 60-nm FET shown in Figure S5(b). The current shows small modulation (I_{on}/I_{off} ~100) with the gate voltage compared with that of a FET chain with an overall gap of 90 nm. This modulation is caused by variation of the MoS_2/metal contact resistance because MoS_2 in the contact region (under the Au electrodes) does not undergo the phase transition and thus remains intact. Given the low resistance of 1T'-phase MoS_2, the total resistance of this device gives a good estimation of the 2H MoS_2/metal contact resistance. These contact characteristics are in good agreement with the respective values that were independently extracted from the fitting model (see Figure S10).

CVD monolayer-MoS_2 FET

Figure S6 (a) shows the transfer characteristics (I_{ds}-V_{gs}) evolution of a 120 nm monolayer MoS_2 FET (ML-MoS_2 FET) to a patterned 2H/1T' ML-MoS_2 FET with a half-pitch of 7.5 nm.

As can be seen in Figure S6 (a), the ML-MoS_2 has survived the PS etching step and still shows high I_{on}/I_{off} modulation. However, current degradation of more than two orders of magnitude is observed as well as a worse SS and shifted subthreshold voltage (V_t) compared with the as-fabricated MoS_2-FET. These changes are the consequences

of the MoS_2 surface being affected by the plasma radicals. The unwanted degradation is nevertheless a direct indication that the PS film is fully etched and the gap between ox-PDMS lines is fully opened and ready for *n*BuLi treatment. We need to consider that a monolayer of MoS_2, used in the device of Figure S6, is the extreme case in this etching process, and obviously a thicker MoS_2 channel would be less affected by the process as the underlying layers would be shielded against the radicals by the topmost layer.

The last I_{ds}-V_{gs} curve in Figure S6 (a) shows the same device characteristics after *n*BuLi treatment. Since 1T' regions are fully metallic, they play a role as contacts to the semiconducting 2H regions under the ox-PDMS cylinders. This configuration effectively presents a chain of transistors in the series mode where each one has a 7.5-nm 2H-MoS_2 channel, seamlessly contacted to 7.5-nm-long 1T'-MoS_2 on both sides as S/D contacts, as shown schematically. The pronounced changes are the increase in current and further degradation of SS. The former change arises from the semiconducting to metallic conversion that decreases the effective channel length and the latter change results from the so-called short channel effect, which will be discussed in detail later in this work. This chain of transistors demonstrates the operation of MoS_2 transistors with the shortest and thinnest channel, that is ~7.5 nm long and ~7 Å thick, reported to date. Figure S6(b) shows the final device at different V_{ds} values highlighting the increase of I_{off} at V_{ds}=1 V, which can be attributed to direct source-drain tunneling. This matter in discussed in more detail in the main text.

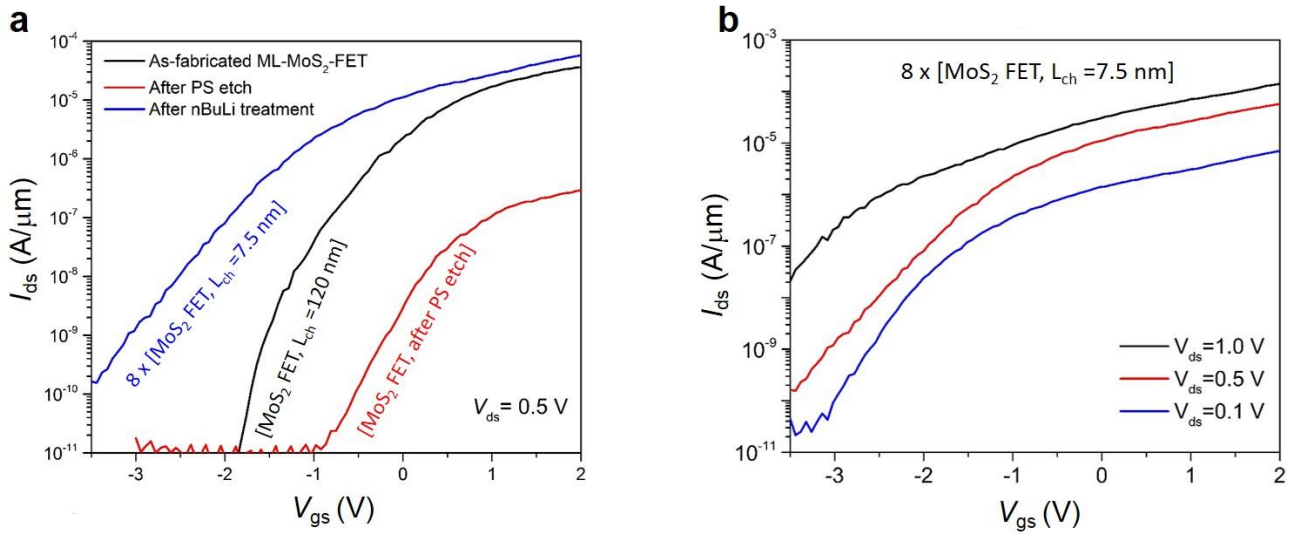

Figure S6. (a) Evolution of a CVD monolayer MoS_2-FET showing I_{ds}-V_{gs} characteristics at V_{ds} = 0.5 V of the as-fabricated (channel length=120 nm), after PS-etch and after phase transition treatment with *n*BuLi. The phase transition treatment converts

the long channel to a chain of short channel transistors in series with a channel length of 7.5 nm connected together with a metallic 1T' MoS_2 junction. (b) I_{ds}-V_{gs} of the final device at different V_{ds} values.

We also tested BCP with a pitch of 43 nm, which provides transistor channels with a nominal length of ~22 nm. Figure S7 compares the transfer and output characteristics of a monolayer MoS_2 device with 215-nm channel length before and after patterning into a chain of five 2H/1T' MoS_2 regions. Similar to the chain of the 7.5-nm MoS_2 FETs, both larger on-current and off-currents are observed along with increased SS. The I_{ds}-V_{ds} curve of the as-fabricated ML-MoS_2 FET shows excellent current saturation, which is distorted after formation of short-channel transistors.

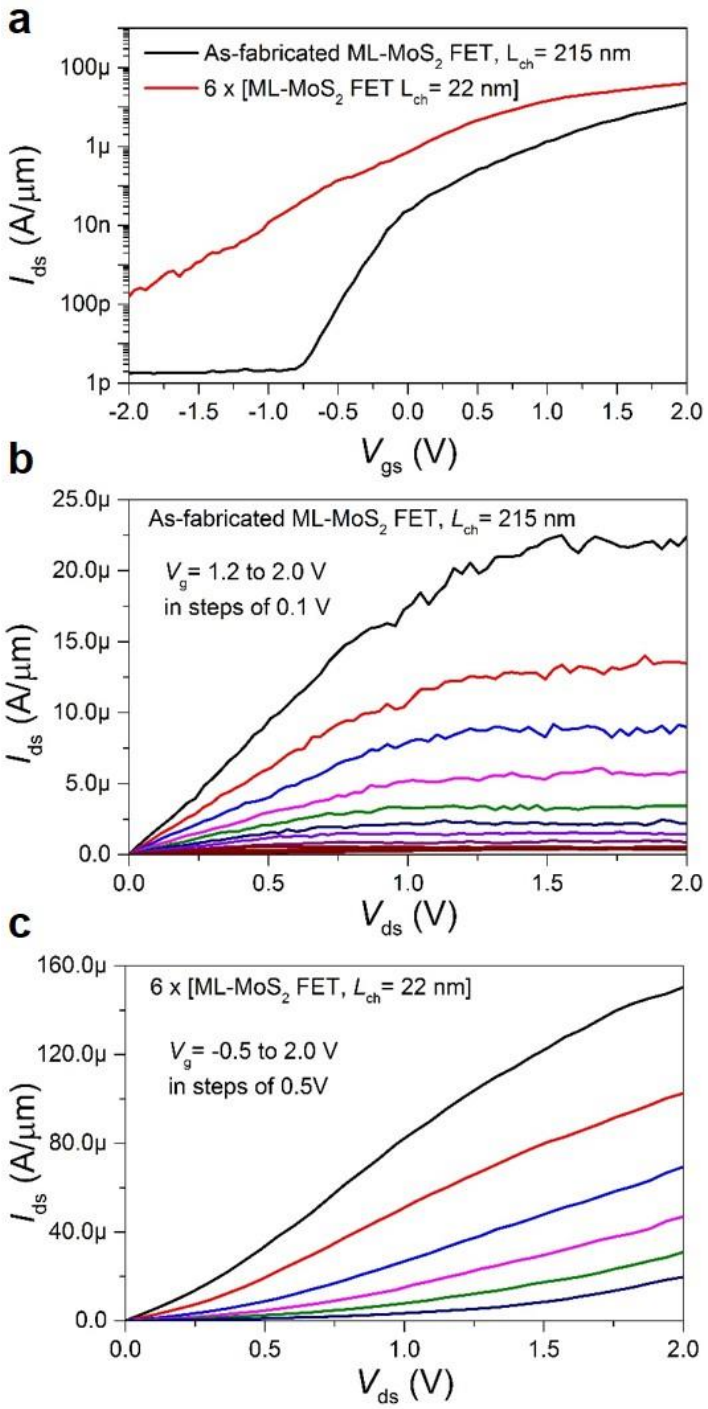

Figure S7. (a) I_{ds}-V_{gs} characteristics of an as-fabricated 215-nm monolayer MoS_2 device and final device with six 22-nm channels in series. (b) and (c) I_{ds}-V_{ds} characteristics of the as-fabricated and final device, respectively.

Details of the MVS and NEGF models:

MVS model:

We briefly describe the transport equations in MVS. Drain current (I_{ds}) is calculated from the following compact expression,

$$I_{ds} = Q_{xo} v_{xo} F_{sat}$$

where Q_{xo} is the charge density at the top of the channel barrier, located at the virtual source (VS) or the injection point near the source contact. Q_{xo} is a primarily determined by the gate voltage V_{gs} and to some extent by the drain bias V_D through a drain induced barrier lowering (DIBL) term, δ. Gate capacitance, C_{ox}, the subthreshold swing parameter n and the threshold voltage parameter V_t decides the shape and transition (from exponential to linear) points of Q_{xo}. v_{xo} is the injection velocity (at the VS point) and F_{sat} is an empirical function that captures the saturation of the drain current with drain bias.

$$F_{sat} = \frac{V_{ds}'}{V_{DSAT}} \Big/ \left(1 + \left(\frac{V_{ds}'}{V_{DSAT}}\right)^{\beta}\right)^{\frac{1}{\beta}}$$

which gradually varies from 0 to 1 as the drain bias is changed from 0 to V_{DSAT} and β is an empirical (typically around 1.4-1.8) parameter to match the shape of the output characteristics. V_{ds}' is the internal applied voltage excluding the voltage drops in the access resistances R_s and R_d.

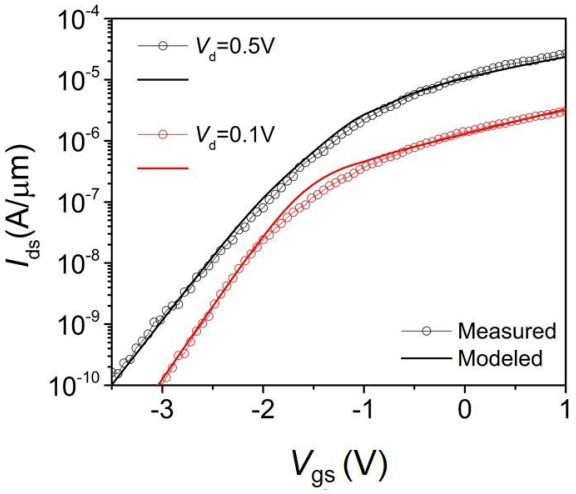

Figure S8. I_{ds} vs V_{gs} characteristics of fabricated MoS_2 FET at different V_{ds} along with MVS fitting of the characteristics.

Figure S8 shows the MVS fitting for the monolayer device. The monolayer devices have a larger DIBL of 0.75 V/V and higher SS (~460 mV/dec.) than their trilayer counterparts, which have a DIBL of 0.7 V/V and SS of 120 mV/dec. These discrepancies can be attributed to a lack of plasma-induced defect states in the channels of the tri-layer MoS_2 devices. The other parameters are mobility μ=12 cm^2/V.s, resistance R=80 Ω.μm and velocity v_{xo}=of 8×10^5 cm/s.

The circuit used in the Advanced Device Simulator (ADS) is shown in Figure S9. In addition to the chain of transistors, two extra transistors (circular blocks) are used with similar MVS parameters to represent V_{gs} dependent R_s and R_d.

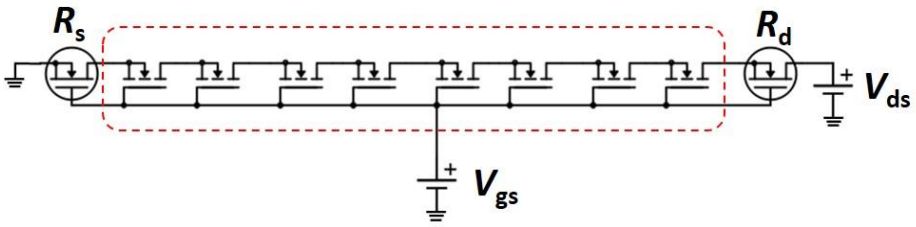

Figure S9. Circuit configuration of the series of FETs used in ADS simulator and corresponding biasing configuration. R_s and R_d are representing the gate voltage dependent contact resistances.

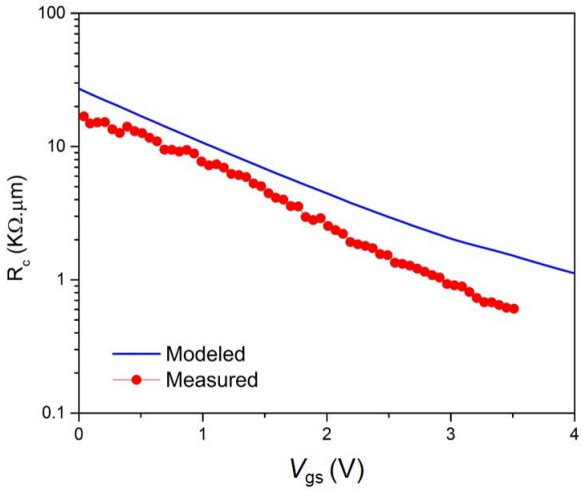

Figure S10. Contact resistance vs. gate voltage from the model and data from a similar device of Figure S9.

Figure S10 shows the contact resistance used to fit the data. The MoS_2 sample has low carrier density at V_{gs}=0 yielding contact resistance ~20 KΩ.μm. Contact resistance decreases below 1 KΩ.μm when the channel is sufficiently populated with carriers. The total contact resistance (blue line) that fits the experimental transfer curve is close to the contact resistance of our MoS_2 device shown in red circles (see the discussion of Figure S5 (b)).

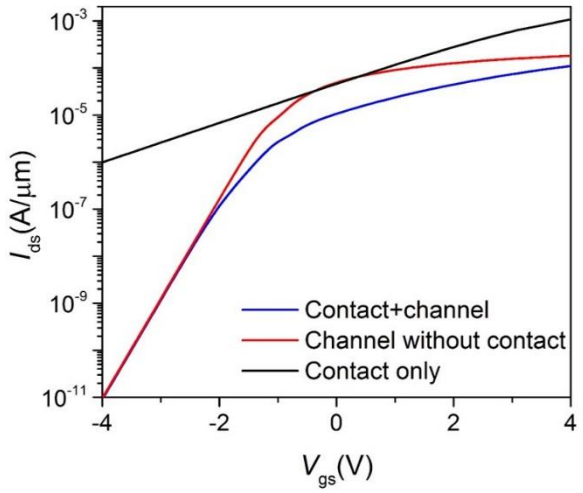

Figure S11. Transfer characteristics of the monolayer device with and without the contact resistance.

Figure S11 shows the effect of the contact resistance on the transfer characteristics. With the contact resistance, the output current increases slowly above threshold and takes a much higher voltage (blue) to saturate than it takes

without the contact resistance (red). The black line shows the current if only the contact were considered in the circuit. Below threshold the current changes exponentially and the transport is controlled by the MoS_2 transistors. But above the threshold ($V_{gs} > -1$ V); the current changes in a superlinear fashion, which results from the contact resistance. At higher voltages (V_{gs}>1V), channel resistance dominates again.

NEGF Simulation details:

The 2D Poisson equation is converted into a 1D equation[6]

$$\frac{d^2\psi}{dx^2} - \frac{\psi - \phi_{gs}}{\lambda^2} = -\frac{\rho}{\epsilon}$$

provided that the effective scaling length is $\lambda = \frac{\sqrt{t_{ox} t_{semi} \epsilon_{2D}}}{\epsilon_{ox}}$. ψ is the surface potential and $\phi_{gs} = V_G - V_{FB}$ is the gate potential. Charge density at each point is calculated from the non-equilibrium Greens function (NEGF) formalism[7],

$$\rho = \frac{q}{2\pi} \int_{E_c}^{\infty} [G\Gamma_S G\, f_S + G\Gamma_D G\, f_D] dE$$

where f_s and f_d are the source and drain Fermi Functions. G is the retarded Green's function calculated at an energy E from,

$$G = (E\mathbf{I} - H + \psi - \Sigma_s - \Sigma_D)^{-1}$$

A single band effective mass Hamiltonian is used from the discretized Schrodinger equation. Effective mass and bandgap parameters are taken from Alam *et al.*[8] Source to channel barrier height is set to $E_g/2$ when V_{gs} = 0. The contact self energy matrices calculated from contact surface Green's function, $g_s = \left((E + \phi_{0,L})I - H - \tau^+ g_s \tau\right)^{-1}$ which is solved iteratively. ϕ_0 and ϕ_L are the boundary potentials for the particular barrier height and drain bias. In order to capture the 2D density of states, a transverse k_y dependent Hamiltonian is used. Transmission and density of states are found by inverse Fourier transforming to the real space[9]. Inversion of the matrices are expedited by using Recursive Green's function Algorithm[10]. The self-energy matrix is found from $\Sigma = \tau^+ g_s \tau$ and the anti-Hermitian components give the broadening matrix Γ. Once the self-consistency is achieved between ρ and ψ, current is calculated from,

$$I = \frac{2q^2}{h} \int Tr[G\Gamma_s G\Gamma_D](f_s - f_d) dE$$

Details of DFT calculations:

DFT calculations were performed using the Vienna *ab initio* simulation package[11] with projector-augmented wave potentials[12, 13]. The generalized gradient approximation parameterized by the Perdew–Burke–Ernzerhof functional [14]

was used as the exchange-correlation functional. The lattice constants of monolayer 1T'- and 2H-phase MoS_2 were obtained *via* structural optimization. The lattice mismatch between the two phases in constructing the 2H/1T' lateral junction was smaller than 0.05%. The vacuum layers were more than 20 Å thick to ensure decoupling between neighboring slabs. The energy cutoff was 450 eV for the plane-wave basis sets. During structural relaxation, all the atoms were allowed to relax until the force on each atom became smaller than 0.02 eV/Å. A Gamma-centered 9×15×1 k-point mesh was used for the $\left(1 \times \sqrt{3}\right)$ cell and one of 1×15×1 was used for the 2H/1T' junction. The adsorption site and configuration of H were carefully examined, and all the calculations were spin-polarized. Figure S12 compares the electronic and atomic structures of 1T and 1T' MoS_2. The 1T' phase is more stable than 1T by 0.29 eV per formula unit, and both phases are calculated to be metallic. Although the 1T' phase is less stable than the 2H phase in the pristine form, as shown in Figure S13, it becomes even more stable with the addition of H or OH. However a small bandgap (E_g < 400 meV) opens up in the electronic structures of the functionalized 1T' MoS_2. Nevertheless, the 1T' phase retains its metallic characteristics upon the adsorption of H or OH groups as the Fermi level is well above the conduction band edge.

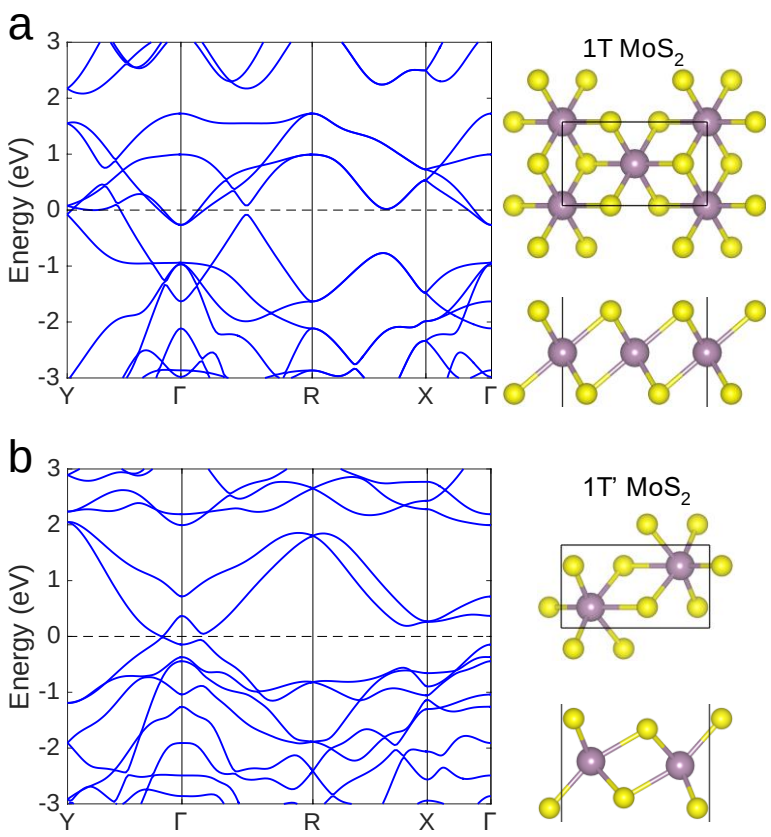

Figure S12. Electronic band structures and atomic structures of 1T (a) and 1T' (b) MoS_2.

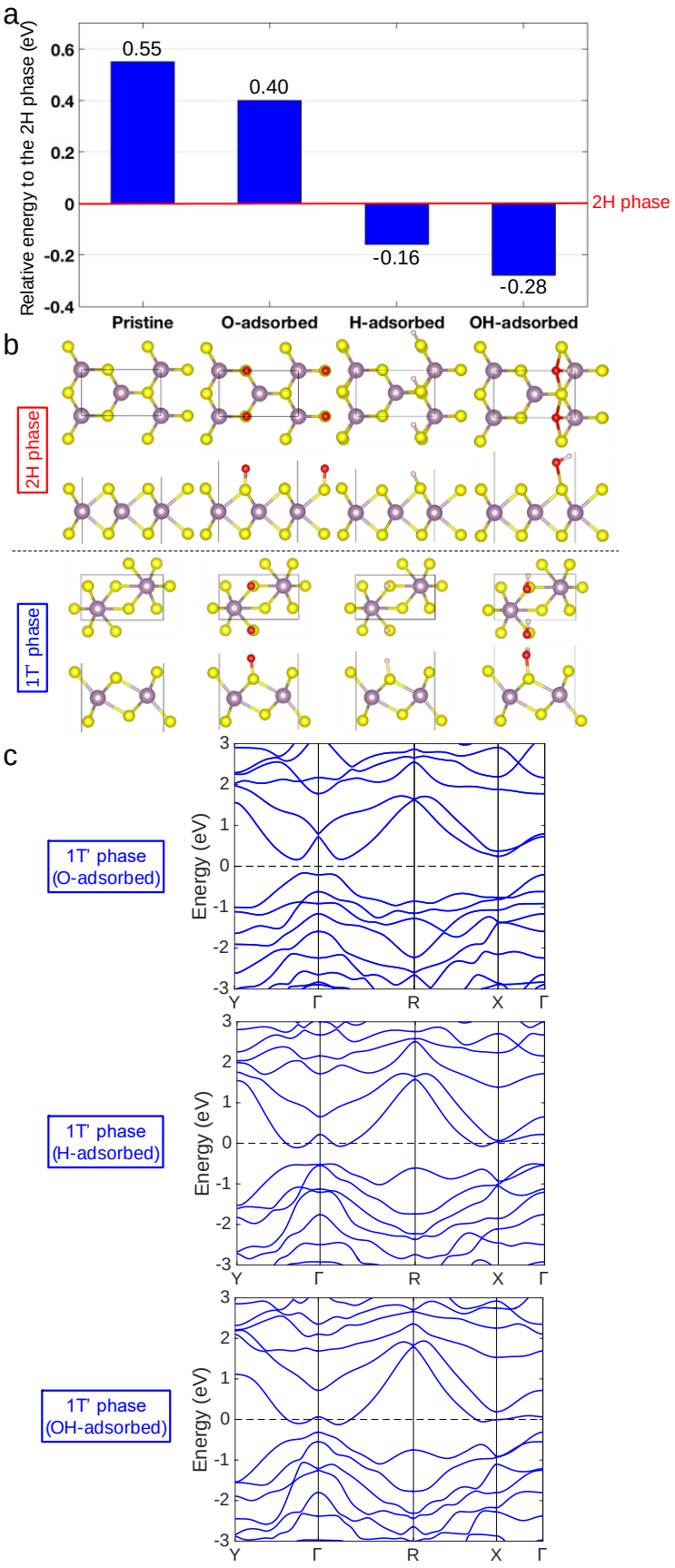
a
Relative energy to the 2H phase (eV)
0.6
0.4
0.2
0
-0.2
-0.4
0.55
0.40
-0.16
-0.28
2H phase
Pristine
O-adsorbed
H-adsorbed
OH-adsorbed
b
2H phase
1T' phase
c
1T' phase
(O-adsorbed)
1T' phase
(H-adsorbed)
1T' phase
(OH-adsorbed)
Energy (eV)
3
2
1
0
-1
-2
-3
Y
Γ
R
X
Γ

Figure S13. (a) The energy per formula unit of the 1T' phase with respect to the 2H phase. Energies of the pristine, O-adsorbed, H-adsorbed, and OH-adsorbed 2H phases are all set to zero as the reference. The negative values mean the 1T' phase is more stable. (b) Top and side views of the atomic structures of the pristine and functionalized 2H and 1T' phases. (c) The band structures of the 1T' phase with the adsorption of functional groups at the coverage of 0.5/Mo.

Figure S14 shows contour plots of partial charge densities associated with the states in the energy range of [E_F−1.0 eV, E_F] at the two boundaries between the 1T'- and 2H-phases. The numbers in the color bar are in units of e/Å^3. The isosurface levels are selected at 0.02 e/Å^3. The partial charge density distribution on the side of the 1T' phase is very similar at the two boundaries

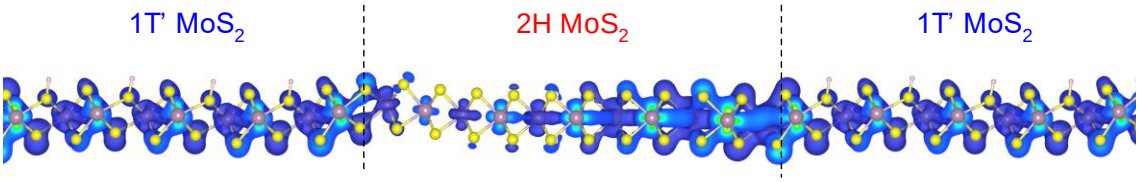

Figure S14. The partial charge density associated with the states in the energy range of [EF-1.0 eV, EF] for the entire device.

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